AIT1168 Video Signal Processor ™ (VSPro) ™

US Patent 5526055

VGA to NTSC/PAL Converter

The AIT1168 Video Signal Processor converts the analog RGB output signals from any VGA compatible graphic signal into analog NTSC or PAL video. Scan rate conversion is accomplished by the integrated memory of the AIT1168 using the AITech proprietary scan conversion algorithm. Advanced *Flic-Free*™ digital filter technology provides a clear and stable video display.

The AIT1168 is a function superset of the AIT1108E and will perform similar to it for the three AIT1108E operating modes. The AIT1168 also provides four additional modes to support full underscan in 640x480 and 800x600 VGA resolutions.

All video processing is done in the digital domain with no tuning circuits. Oversampling techniques in the digital encoder result in very simple and inexpensive analog output filters. Both composite (single lead) and S-Video (separate chroma and luma) formats are generated simultaneously by the three 10-bit output DACs, each of which generates a standard video-level signal into a 50Ω load (150Ω termination at the source and 75Ω load at the video monitor).

The AIT1168 requires an absolute minimum of external components. Precision timing is derived from a single 27 MHz crystal or clock reference. All control is via package pins, and no additional micro-controller is required. Video and filtering modes may also be selected through software by programming the VSYNC timing.

The AIT1168 supports the VESA DPMS power down mode to conserve power. The operational state of the AIT1168 is controlled by the pulse activity on VGA HSync and VGA VSync (refer to *Table 2*).

The AIT1168 is fabricated in a sub-micron CMOS process and packaged in the 80-Lead MQFP.

Product Information

Features

- Single chip crystal-controlled All-Digital Video Signal Processing
- Supports 640 x 480 and 800 x 600 overscan and underscan
- Three 8-Bit A/D Converters for input signal conversion
- Three 10-bit D/A Converters for output
- Supports NTSC, NTSC-EIAJ, and PAL B/G/I standards
- I^2C-bus Interface
- Supports VESA DPMS or hardware power-down mode
- Anti-Flicker filtering
- Control pins determine Set-up No microprocessor required
- Simultaneous S-Video and Composite video outputs
- Single +5V power supply

Applications

- Internet Appliances
- Intercast
- Internet-ready TV/Set-Top boxes
- Advanced VGA to Video Converter Add in Cards.
- Embedded Desk-Top and Portable computers with TV out.
- 3-D Graphic/Game application

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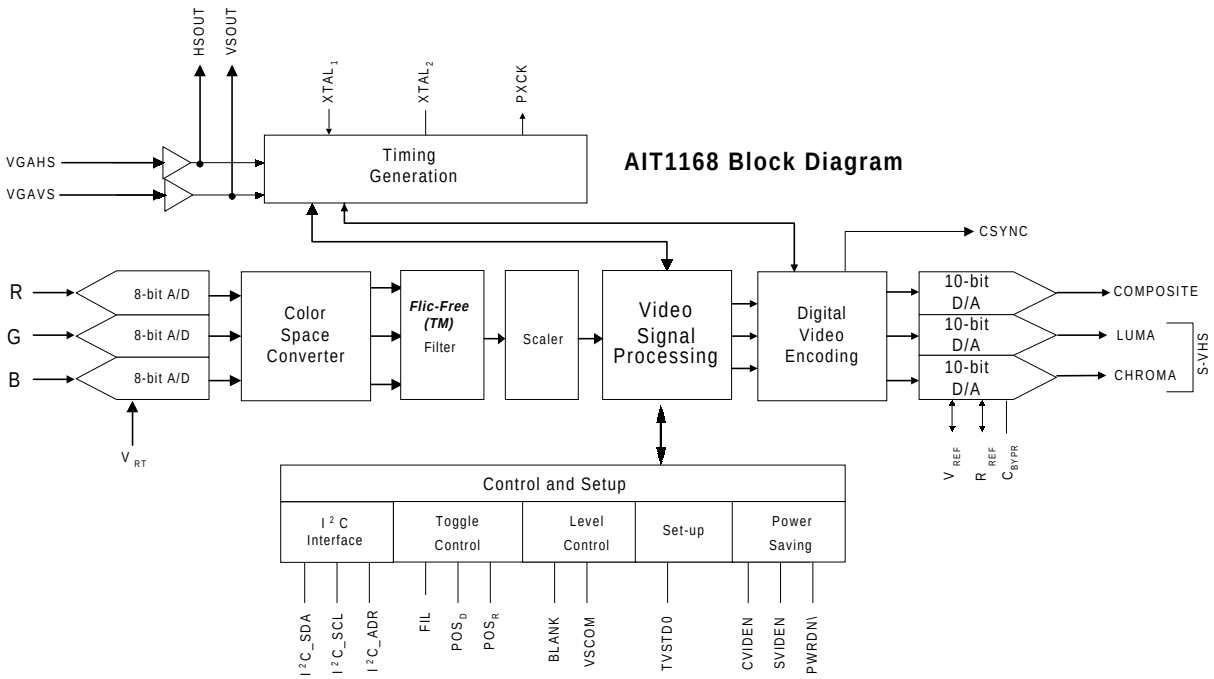

General Description

The AIT1168 comprises all of the circuitry necessary to convert the analog RGB signal from a graphic controller or RAMDAC into standard base band video adhering to worldwide NTSC and PAL standards.

The AIT1168 is a totally-integrated graphic-to-NTSC/PAL processor with simultaneous composite and Y/C (S-Video) outputs. Using the internal line cache provides anti-flicker conversion with VGA input at 2x the TV refresh rate.

The AIT1168 operates entirely in the digital domain except for A/D conversion of the graphic input signals and D/A converters that output composite and S-Video signals.

Operation

The analog VGA signal is digitized by three A/D converters. The standard signal range is from 0 to 0.85V, and other value could be accommodated by changing the reference voltage.

Clocks for the input portion of the AIT1168 are generated by an internal phase-locked loop with an integral divide-by-N counter. This clock generator uses the VGA horizontal sync as its input reference frequency. The clock generated by the PLL and counter is locked to the incoming line rate, and is used to digitize a fixed number of pixels per line.

Vertical timing information is derived from VGAVS, the vertical sync signal from the VGA controller. This synchronizes the video encoder with the incoming signal. HSYNC and VSYNC may be of either polarity: the AIT1168 automatically determines and accommodates any combination. Operational commands may be conveyed from the PC to the chip over the VGAHS and VGAVS signals such as DPMS, VSCOM controls, for example.

Input A/D conversion

Eight-bit A/D converters are used on each of the red, green, and blue input video signals at up to 40MHz sampling rate. HSYNC and VSYNC are similarly buffered by Schmitt trigger gates. Typical RGB signal ranges from 0 to 0.85V, however, the A/D converters are operating below their optimal. A different reference voltage can be applied to V_{RT} and will override the internal reference. This externally supplied reference voltage should be equal to the maximum RGB signal range.

Converting from RGB to Components

Digital video processing within the AIT1168 is done with common YUV color components. The output of the RGB-to-YUV matrix is in 24-bit YUV data. For convenience and efficiency,

the YUV digital video data is decimated to 4:2:2 format.

Anti-Flicker Filtering

To reduce flicker due to single line elements of the graphic input image and the interlace structure of NTSC and PAL video, a finite impulse response digital filter is used. This is constructed using the proprietary AITech algorithm.

Scan Conversion Operation

The AIT1168 front end comprises all circuitry in the signal path from the A/D converters through the vertical filter network. All front end circuits operate at the phase-locked clock frequency. The internal FIFO devices perform scan rate conversion and provide line delay for filter logic.

When the flicker filter is turned on, up to four lines of data from the input frame are used to generate one line of output frame. On each odd field, only odd lines of the output frame are written into the data buffer FIFO devices. Similarly, on each even field, only even lines of the output frame are written into the data buffer FIFO devices.

In overscan mode, the input frame is not scaled. The digital processor generates a flicker filtered output frame at the same resolution as the input frame. The horizontal scan rate is exactly twice the output scan rate in this mode. The 1:1 aspect ratio is preserved.

In underscan mode, the input frame is scaled down such that the complete output frame can be displayed on the television. The horizontal and vertical scaling factors for NTSC and PAL modes are adjusted to preserve a 1:1 aspect ratio.

The AIT1168 supports seven different input modes, each mode requires a certain fixed number of lines per frame. No mode selection pin is necessary. The internal logic detects the input modes by counting the number of lines per frame. If the number of lines does not match one of the seven modes, the default 640x480 overscan NTSC output mode is used.

Horizontal and vertical synchronization signals are digitally generated by the AIT1168 with controlled rise and fall times on all sync edges, the beginning and end of active video, and the burst envelope. All elements of horizontal and vertical sync timing as well as sub-carrier frequency and phase are preset. The AIT1168 will auto-detect NTSC/PAL by counting the number of input lines per frame. Control pin ($TVSTD_0$) selects between the NTSC and NTSC-EIA standards.

The AIT1168 will handle 7 different VGA modes, each mode requires a different number of lines per frame. The VSCOM is kept compatible with the AIT1108E in setting the filter mode and the screen blank function.

Positioning

There are two positioning function pins that allow the encoded graphic image to be shifted up/down and left/right. This is to ensure that borders and menu bars are visible in the active picture area of the NTSC/PAL output.

Internal Digital Video Encoder

The processor section of the AIT1168 accepts digital video data in YUV4:2:2 format from the color space converter. The processor input is separated into luminance and chrominance components. The chrominance signals are used to modulate a digitally synthesized sub-carrier. The luminance and chrominance signals are separately interpolated to twice the pixel rate, and converted to analog S-Video signals by 10-bit D/A converters. The analog composite video signal is output by a third 10-bit D/A converter

Encoder Timing

The AIT1168 digital encoder module operates from the same clock used in the input section. A 27 MHz clock signal is used to generate the reference sub-carrier frequency. Alternately, another reference clock input frequency such as 14.318MHz can be used to generate the reference sub-carrier frequency. This 24-bit value for the sub-carrier frequency adjustment needs to be input via the I^2C interface.

Blanking

The AIT1168 is designed to enable blanking the screen to blue from the control input. By setting BLANK to HIGH, the video screen will be set to blue.

Underscan Selection

The sampling default setting is in overscan, 640 x 480 mode. This provides a square pixel conversion from VGA to video. For other modes, different VGA timings must be provided to the AIT1168. The AIT1168 auto-detects the new frequencies and establishes the proper operating mode. *Table 1* summarizes the VGA and TV timings of all the seven modes that AIT1168 supports.

Table 1: VGA and TV Timing Summary

	VGA Timings						
	Overscan	**Underscan**	**Overscan**	**Underscan**	**Underscan**	**Overscan**	**Underscan**
Active screen area	640x480	640x480	640x480	640x480	800x600	800x600	800x600
Pixel/Line	800	784	864	944	880	944	1000
Line/Frame	525	600	625	625	735	625	750
VS	59.94	59.94	50	50	59.94	50	50
HS(kHz)	31.4685	35.964	31.25	31.25	44.0559	31.25	37.5
Pixel clock (MHz)	25.1748	28.195776	27	29.5	38.769192	29.5	37.5
	TV Timings						
System	**NTSC**	**NTSC**	**PAL**	**PAL**	**NTSC**	**PAL**	**PAL**
Visible VGA Resolution	600x426	640x480	640x480	640x480	800x600	692x535	800x600
Line/Frame	525	525	625	625	525	625	625
VS	59.94	59.94	50	50	59.94	50	50
H scale ratio	1:0.975	1:0.87	1:0.91	1:0.83	1:0.87	1:1.04	1:0.82
V scale ratio	1:1	1:0.875	1:0.83	1:0.83	1:0.89	1:1.04	1:0.87
	Default power-up mode. Same as AIT1108			Same as AIT1108 Mode		Same as AIT1108 Mode	

D/A Converters

The analog outputs of the AIT1168 are the outputs of three 10-bit D/A converters. The outputs are capable of driving standard video levels into 50 Ohm (150 Ohm termination at the source and 75 Ohm load at the video monitor) loads. The AIT1168 has an internal 1.25 Volt reference voltage, V_{REF}, to provide the reference voltage for the three D/A converters. The R_{REF} resistor value should be 140 Ohms.

Power Conservation

The AIT1168 supports the VESA DPMS power down mode to conserve power. The operational state of the AIT1168 is controlled by the pulse activity on VGA HSync and VGA VSync according to *Table 2*. Because the VGA HS is used to detect the proper operating mode, the "Stand-by" mode in which the VGA switches off the HS cannot be supported.

Table 2: Supported DPMS Modes Summary

DPMS State	VGA HSync	VGA VSync	AIT1168 state
On	active	active	On, video active
*Stand-by**	*inactive*	*active*	*This mode is not supported*
Suspend	active	inactive	Suspend, screen blanked A/D and front-end powered down
Off	inactive	inactive	Off, AIT1168 powered-down

When the AIT1168 is not in use, it can conserve power further by using the PWRDN\ pin. When recovering from power-down, AIT1168 retains all the prior settings.

I²C-Interface Operation

The AIT1168 provides an I²C interface capability which simplifies both the design and operation of the product. The AIT1168 I²C bus uses two bi-directional wires, serial data (SDA) and serial clock (SCL) to transfer information between devices connected to the bus. Each device is recognized by a unique address. The AIT1168 I²C interface is only for slave mode so that the clock for synchronizing data transfer is generated by an I²C master. There are ten accessible I²C control registers. Writing to these control registers will override all other hardware or software control. Asserting chip reset causes the AIT1168 to regain set-up controls via hardware or software.

I²C Interface Characteristics

1. Serial data and clock rate up to 100K Hz.
2. Always in slave mode.
3. All registers are write only.
4. Each access must include 8-bit sub-address.
5. No response to general calls.

I²C Input Pin

The AIT1168 I²C interface is controlled by four hardware pins.

- I²C_En\ : The state of this pin enables (logic low) or disables (logic high) the I²C control logic. It shares the same pin with PWRDN\.
- I²C_SDA : I²C serial data input pin.
- I²C_CLK : I²C serial clock input pin.
- I²C_ADR : This pin select one of the slave device addresses.

I²C Device Address

The I²C interface responds to the slave device address selected by the I²C_ADR pin.

I²C_ADR	Slave Device Address
0	10001000 (88h)

I²C Sub-Address

The I²C Interface writes to one of the ten control registers. These control registers control various function of the chip. The control register data will override current hardware or software setting. Each I²C access must include one of these sub-addresses defined in this section. The user must use the correct sub-address; otherwise, the AIT1168 might lock into a wrong operating state.

Sub-Address	Register Definition
6	Horizontal Position Register
7	Vertical Position Register
8	Encoder Control Register
9	Input Control Register
3	Fsc Frequency Control Register
4	Fsc Frequency Control Register
5	Fsc Frequency Control Register
B	PLL Control Register
C	PLL Control Register
D	Setup Register

I²C Write Cycle Format

The AIT1168 I²C interface supports only write cycle operation by the master device. Each write access to one of the ten control registers has the following transfer protocol:

Start	Slave Address	Write	Ack	Sub-address	Ack	Data	Ack	Stop

Start : The start condition is defined as the falling edge of the SDA signal while SCL (serial clock) is high.
Slave Address : It is the 7-bit slave device address used by the AIT1168. Upon communication established, the AIT1168 expects a device address ID from the master device. This device address is determined by the state of the I²C_ADR pin.
Write : This bit is always "0" because the I²C interface is write only.
Ack : This bit is the acknowledge bit. The AIT1168 pulls the SDA data line to logic "low" to acknowledge successful reception of the 8-bit data.
Sub Address : It is the 8-bit sub-address for accessing to one of the four control registers.
Data : This is the 8-bit value to be written into the control register.
Stop : The stop condition is initiated to terminate the I²C communication. It is defined as the rising edge of SDA signal while SCL is logic "high". Figure 1 shows a typical I²C interface transfer protocol of the AIT1168.

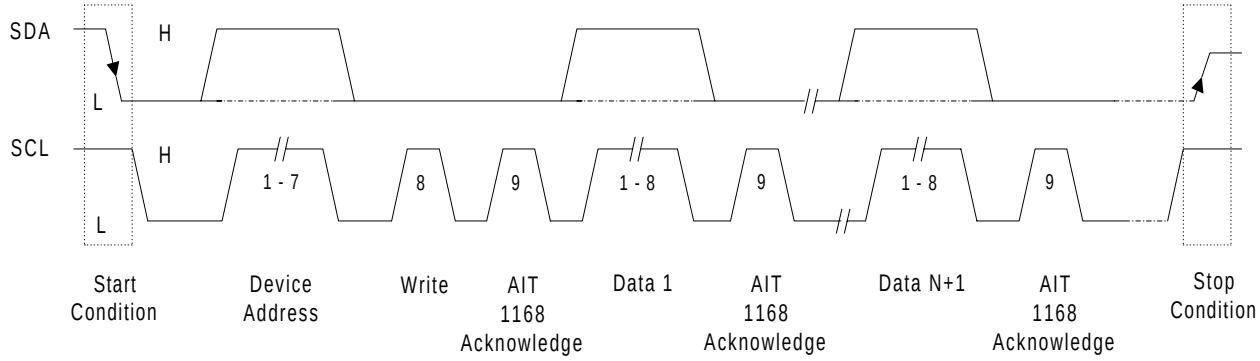

Figure 1. Serial Communication Port Transfer Protocol

Once the I²C interface updates a control register. The contents of the control register will override other external hardware or software controls. Once written, the I²C control information can only be changed by writing new information via the I²C port or by asserting the reset pin of the AIT1168. Access to each control register must start with the START condition and end with the STOP condition.

I²C Register Definition

Horizontal Position Register **Address : 06H**
Bits : 8

The 8-bit binary value defines the horizontal position of the output video image. The 8-bit value is a 2s-compliment number. Each operating mode has its own startup default value. Subtracting from the start up default value will move the screen to the right. Adding to the start up default value will move the screen to the left. Each step represent 2-pixels. Since it is a signed-value, the most significant bit of this register is the sign bit. The start up default value for each operating mode are as followed:

Mode	Default Value
640x480 overscan NTSC	10000100 (binary)
640x480 underscan NTSC	10000100 (binary)
800x600 underscan NTSC	00111100 (binary)
640x480 overscan PAL	10000100 (binary)
800x600 overscan PAL	01101100 (binary)
640x480 underscan PAL	10000100 (binary)
800x600 underscan PAL	01101100 (binary)

Note that writing into this control register will override the current setting. The horizontal position hardware pin is disabled until the chip is reset.

Vertical Position Register **Address : 07H**
Bits : 8

The 8-bit binary value defines the vertical position of the output video image. The 8-bit value is a 2-compliments signed number. Each operating mode has its own startup default value. Subtracting from the start up default value will move the screen downward. Adding to the start up default value will move the screen upward. Each step represent 1 pixel. Since it is a signed-value, the most significant bit of this register is the sign bit. The start up default value for each operating mode are as followed:

Mode	Default Value
640x480 overscan NTSC	01110100 (binary)
640x480 underscan NTSC	01110100 (binary)
800x600 underscan NTSC	01110100 (binary)
640x480 overscan PAL	01110100 (binary)
800x600 overscan PAL	01110100 (binary)
640x480 underscan PAL	01110100 (binary)
800x600 underscan PAL	11010100 (binary)

Note that writing into this control register will override the current setting. The vertical position hardware pin is disabled until the chip is reset.

Encoder Control Register **Address : 08H**
Bits : 8

Bit:	7	6	5	4	3	2	1	0
Type	W	W	Reserved	W	W	W	Reserved	Reserved

This register controls the encoder function:

bit	description	
7	Color Bar Enable:	1 = Enable color bar output 0 = Normal output
6	Blank:	1 = Blank output 0 = Normal output
5	Reserved:	Default is 1
4	NTSC-EIA:	1 = Select NTSC-EIA output 0 = Select NTSC output
3	UV_SEL:	1 = Normal color processing 0 = Swap U,V color processing
2	Sub-carrier out:	1 = Enable Sub-carrier signal on chroma output 0 = Normal chroma output
[1..0]	Reserved:	Must be zeros

Input Control Register **Sub Address : 09H**
Bits : 8

Bit:	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	Reserved

This register controls the input function:

bit	description	
[7..5]	Operating Mode:	000 = 640x480 overscan NTSC 001 = Not valid mode 010 = 640x480 underscan NTSC 011 = 800x600 underscan NTSC 100 = 640x480 overscan PAL 101 = 800x600 overscan PAL 110 = 640x480 underscan PAL 111 = 800x600 underscan PAL
[4..3]	Flicker Filter Mode:	00 = 3 line filter 01 = 2 line filter 10 = No filter 11 = No filter
2	Power Down:	0 = Normal operation 1 = Power down
1	Color Bar Enable:	0 = Normal operation 1 = Enable color bar
0	Reserved	Must be zero

Note that writing into this control register will disable the auto-detect function of operating mode and flicker filter mode. The auto-detect function is enabled again after reset is asserted.

Fsc Freq. Control Registers **Sub Address : 03H, 04H, 05H**
Bits : 24

These registers contain the 24-bit value for the sub-carrier generator. This 24-bit value affects the frequency of the sub-carrier. Definition of the registers are as followed:

Sub-address 3 : T[23..16]
Sub-address 4 : T[15:8]
Sub-address 5 : T[7:0]

Using a 27 MHz reference clock, the 24-bit value for
NTSC = 21F07B hex (default NTSC)
PAL = 2A098A hex (default PAL)

Alternatively, if a 14.31818 MHz reference clock is used, the 24-bit value for
NTSC = 3FFFFF hex (default NTSC)
PAL = 4F4531 hex (default PAL)

IF a different reference frequency is used, the 24-bit value has to be recalculated based on the following equation:

Fsc Freq. Register = (Sub-carrier frequency / Reference frequency) * 2^24;

PLL Control Registers **Sub Address : 0BH, 0CH**
Bits : 8

Bit:	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

These registers contain the divided by N count of the PLL. The value stores in these registers is the actual modulus subtracted by 2. The registers content should not be modified. Modifying these registers will affect the input mode auto-detect function.

Sub-address B :

bit	**description**
[7..6]	Sub-phase[1:0]
5	FEB2_D2 (connected to VCC in latest revision)
4	FEB1_D2
3	OUT_D2 (connected to VCC in latest revision)
2	PRE_DE
[1..0]	PLL_F[9:8]

Sub-address C : least significant bits (LSBs) of a 10-bit divided by N count

bit	**description**
[7..0]	PLL_F[7:0]

Setup Register **Sub Address : 0DH**
Bits : 8

Bit:	7	6	5	4	3	2	1	0
Type	Reserved	Reserved	W	Reserved	W	W	W	Reserved

This register overrides the hardware control pins of the AIT1168.

bit	**description**	
7	Reserved:	Must be zero
6	Reserved:	Must be zero
5	2/4 Position:	1 = Select four positions control 0 = Select two (down and right) positions control
4	Reserved:	Default is 1
3	Phase (select clock phase to run the ADCs):	1 = Falling edge of PXCLK 0 = Rising edge of PXCLK
2	UV_SEL:	1 = Normal color processing 0 = Swap U, V color processing
1	TVSTD0:	1 = NTSC 0 = NTSC-EIA
0	Reserved:	Must be zero

Package Interconnections

Signal Type	Name	Function	Type/ Value	Package/Pin MQFP
Clock	PXCK	Encoder Clock Output	TTL	12
	$XTAL_{1-2}$	Sub-carrier Reference Clock	-	69, 70
	PLL_{LPF}	LPF connect pin for internal PLL	-	64
Global	$TVSTD_0$	Video Output Standard Select	$CMOS_P$	40
	FIL	Flicker Filter Mode Select	TTL_S	42
	VSCOM	Vertical Sync Communications Enable	$CMOS_P$	44
	PWRDN\	Power-Down Control	$CMOS_P$	72
	RESET\	Reset	$CMOS_P$	71
	PHASE	Sampling Phase Control	$CMOS_P$	6
Encoder Controls	CVIDEN	Composite Video D/A Power Enable	$CMOS_P$	74
	SVIDEN	S-Video D/A Power Enable	$CMOS_P$	73
	BLANK	Blank Screen Generator	$CMOS_P$	38
	$POS_{R, D}$	TV Image Position Controls	TTL_S	47, 48
Video Inputs	R, G, B	Analog RGB inputs	0.85 V p-p	59, 53, 50
	V_{TIN}	A/D Converter Reference Input, Buffered	+0.85V	57
	V_{TOUT}	A/D Converter Reference Output, Buffered	+0.85V	56
	V_{RT}	A/D Converter Reference Input, Unbuffered	+0.85 V	55
	VGAHS	VGA Horizontal Sync	TTL_S	46
	VGAVS	VGA Vertical Sync	TTL_S	45
Video Outputs	COM-POSITE	NTSC/PAL Video Output	1 V p-p	2
	LUMA	Luminance-only Video	1 V p-p	80
	CHROMA	Chrominance-only Video	1 V p-p	78
	HSOUT	Buffered VGAHS Output	TTL	27
	VSOUT	Buffered VGAVS Output	TTL	26
	CSYNC	Composite Synchronization Signal Output	TTL	67
Encoder Reference	V_{REF}	Voltage Reference Input	+1.25 V	4
	R_{REF}	Current-setting Resistor	140Ω	3
	C_{BYPR}	Reference Bypass Capacitor	0.1 µF	77
Power	V_{DD}	Digital Power Supply	+5.0 V	7, 9, 14, 29, 33, 34, 35, 62
	V_{DDA}	Analog Power Supply	+5.0 V	51, 52, 60, 75, 76
	V_{DDPLL}	Internal Phase Locked Loop Power	+5.0 V	65
I^2C-bus	I^2C_SDA	I^2C Serial Data Input (logic "high" or logic "low")	TTL Tri-State	10
	I^2C_SCL	I^2C Serial Clock Input (< 400 K Hz)	TTL	13
	I^2C_ADR	Slave Device Address Select	TTL	24

Signal Type	Name	Function	Type/ Value	Package/Pin MQFP
	I^2C_En\	I^2C control logic enable	$CMOS_P$	72
GROUND	DGND	Digital Ground	0.0 V	5, 8, 15, 18, 19, 20, 21, 22, 23, 25, 28, 30, 31, 32, 36, 37, 43, 61
	AGND	Analog Ground	0.0 V	1, 49, 54, 58, 66, 79
	GND_{PLL}	Internal Phase-Locked Loop Ground	0.0 V	63
No Connect	NC	Do Not Connect		11, 16, 17, 39, 41, 68

$CMOS_P$ = CMOS with light pull-up

TTL_S = TTL with Schmitt Trigger

Signal Definitions

A/D Converter Interface

R, G, B — Red, Green, Blue analog input from graphic card/computer. The expected voltage range of these input signals is from 0.0 to 0.85 Volts.

VGAHS — Horizontal sync input from Graphic controller. The polarity of VGAHS is internally corrected to active LOW whether the incoming VGAHS is active HIGH or active LOW. This input may need to be low-pass filtered. A 33Ω resistor with a 10pF capacitor R-C filter is recommended.

VGAVS — Vertical sync input from Graphic controller. The polarity of VGAVS is internally corrected to active LOW whether the incoming VGAVS is active HIGH or active LOW. For embedded design, a R-C filter with 150Ω resistor and 270pF capacitor at VGAVS is required. For external scan converter box design, a 74LS74 Dual D Flip-Flop at incoming VGAVS is required (refer to schematic of Application Note 12).

V_{RT} — A/D reference in, unbuffered. This pin should be connected to a voltage follower or V_{TOUT} pin.

V_{TIN} — Input to top reference voltage buffer. External 0.1uF bypass capacitor should be used.

V_{TOUT} — Top reference voltage buffer output that may be connected to V_{RT} to supply current to A/D converter reference resistors. In power down mode, V_{TOUT} drops to zero.

Clock Generators

PXCK — Output of the line locked PLL clock generator for the A/D and digital encoder. This signal is synthesized from the internal PLL. Refer to Table 1 for pixel clock frequency of each input format.

XTAL1/2 — Connection points for the 27 MHz oscillator/crystal. A stable 27MHz externally generated clock (oscillator) may be fed into $XTAL_1$. With a selected value of capacitors (depends on the characteristic of the crystal) and connecting to a two-terminal crystal between them will generate a stable 27 MHz clock for the processor section of the AIT1168. This clock may be fed into $XTAL_2$.

PLL_{LPF} — Internal phase-locked loop filter node. An external RC network is connected to this pin. The recommended configuration of the loop filter is a 56K Ohm resistor in series with a 0.22 uF capacitor and these two components are parallel to a 2200 pF capacitor to V_{cc} near pin 65. Refer to Application Note 12 for design suggestion.

AIT1168 Controls

$TVSTD_0$ Video output standard select. The AIT1168 auto-detects the incoming VGA frequency and the input line per frame to determine between NTSC and PAL. $TVSTV_0$ sets the video standard between NTSC and NTSC-EIAJ. Refer to *Table 3* for $TVSTD_0$ select.

Table 3: $TVSTD_0$ Select VS. TV Standards

$TVSTD_0$	Video Field Rate	Television Standard
0	60Hz	NTSC-EIA
1	60Hz	NTSC
x	50Hz	PAL/B, G, I

FIL Vertical Filter Mode select (state machine). The 3-line flicker reduction filter may be configured for 3-line filtering, 2-line filtering, and no vertical filtering modes with these pins. If VSCOM is high, FIL will be ignored. Refer to filter modes listed in *Table 4*.

Table 4: Filter Modes

Filter Mode (VSCOM=0)
3-line
2-line
No filter (1-line)
Color Bars

VSCOM Vertical Sync. Communications enable. When HIGH, vertical sync pulse width (VGAVS) will control the filter mode, and FIL will be ignored. The pulse-width will be interpreted according to *Table 5* on page 14.

PWRDN\ When LOW, the AIT1168 is configured for minimum power consumption with all A/D, D/A, and logic disabled. When HIGH, the AIT1168 is fully operational and subject to control input pins. It shares the same pin with I^2C_EN\.

Encoder Controls

BLANK When HIGH, the BLUE color is selected and displayed on the screen until BLANK goes LOW. When LOW, composite and S-video output is available.

POS_D, POS_R Adjust screen position when HIGH. The position controls change the processor timing relative to incoming video so that the viewed image may be shifted right or down, to reveal portions of the image that may be found near the edges or in the over scan areas. Vertical position is adjusted 4 lines per frame, total of 64 lines. While horizontal position is moved 4 pixels per frame, total 64 pixels. Upon reaching the end, the video image will revert to the upper/left most position.

Table 5: VSCOM Summary

VGA Mode	$TVSTD_0$	Video Standard	Video Size	Line/Frame	HS/VS (VSCOM=1)			
					Filter:3-L	Filter:2-L	Filter:1-L	Blank
640 x 480	0	NTSC-EIA	Overscan	525	2	4	5	13
	1	NTSC	Overscan	525	2	4	5	13
640 x 480	0	NTSC-EIA	Underscan	600	2	4	5	13
	1	NTSC	Underscan	600	2	4	5	13
640 x 480	x	PAL	Overscan	625	2	4	5	13
640 x 480	x	PAL	Underscan	625	6	7	9	13
800 x 600	0	NTSC-EIA	Underscan	735	2	4	5	13
	1	NTSC	Underscan	735	2	4	5	13
800 x 600	x	PAL	Overscan	625	10	11	12	13
800 x 600	x	PAL	Underscan	700	10	11	12	13

Encoder Interface

V_{REF} This pin is the output of an internal 1.25 Volt band-gap type voltage reference and provides the required reference voltage for the three D/A converters.

R_{REF} A resistor of 140 Ohms is connected between the R_{REF} terminal and ground to set up the reference current for the three internal D/A converters. The value of this resistor determines the full-scale output current (and therefore the peak video level) of the D/A converters.

COM-POSITE This analog base band composite video output can drive 1 Volt peak-peak video into a 50 Ohm terminated line. The composite signal contains all sync, sub-carrier and active video information to drive monitors, projectors, VCRs or other video input devices.

LUMA This analog base band monochrome video output can drive 1 Volt peak-peak video into a 50 Ohm terminated line. The luminance signal contains all sync and active video information necessary to drive black-and-white video input devices.

CHROMA This analog chrominance video output drives a 50 Ohm terminated line. The CHROMA signal, when combined with the LUMA output signal comprises an S-Video two-wire video signal and is suitable for driving monitors, projectors, VCRs and other S-Video input devices.

C_{BYPR} An external 0.1 µF capacitor should be connected between C_{BYPR} and V_{DDA} to reduce noise on the internal reference circuitry.

Power and Ground

V_{DD} +5 Volt power to internal digital circuits.

V_{DDA} +5 Volt power to internal analog circuits. V_{DD} and V_{DDA} must come from the same source.

DGND Ground point for internal digital circuits.

AGND Ground point for internal analog circuits. D_{GND} and A_{GND} should be connected to the same ground plane.

Note: Table 7 on page 21 and 22 provides a function comparison reference for the AIT1168 and AIT1108.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Power Supply Voltages

- V_{DDA} (Measured to AGND) ..... -0.5 to +7.0V
- V_{DD} (Measured to DGND) ..... -0.5 to +7.0V
- V_{DDA} (Measured to VDD) ..... -0.5 to +0.5V
- A_{GND} (Measured to DGND) ..... -0.5 to +0.5V

Digital Inputs

- Applied Voltage (Measured to DGND)[2] ..... -0.5 to V_{DD}+0.5V
- Forced current [3, 4] ..... -10.0 to +10.0 mA

Analog Inputs

- Applied Voltage (Measured to AGND)[2] ..... -0.5 to V_{DDA}+0.5V
- Forced current [3, 4] ..... -10.0 to +10.0 mA

Outputs

- Applied voltage (Measured to DGND)[2] ..... -0.5 to V_{DD} + 0.5V
- Forced current [3, 4] ..... -6.0 to +6.0 mA
- Short circuit duration (single output in HIGH state to ground) ..... 1 second

Temperature

- Operating, ambient ..... 0 to 70°C
  - junction ..... +140°C
  - case …….. +125°C
- Storage ..... -20 to +70°C

Electrostatic Discharge[5] .....±150 V

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Digital Power Supply Voltage	4.75	5.0	5.25	V
V_{DDA}	Analog Power Supply Voltage	4.75	5.0	5.25	V
A_{GND}	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
F_{xtal}	Crystal/Reference Clock Frequency		27		MHz
f_{XTOL}	Crystal/Reference Clock Frequency Tolerance	0	±300	±810	Hz
f_H	VGAHS Frequency in overscan mode				
	59.94 Hz Modes		31.469		KHz
	50Hz Modes		31.250		KHz
N_H	Lines per VGA field in overscan mode				
	59.94 Hz Modes	525	525	525	
	50Hz Modes	625	625	625	
	Tolerance	±0	±0	±0	
t_{PWH}	Reference Clock Pulse Width, HIGH		18.5		ns
t_{PWL}	Reference Clock Pulse Width, LOW		18.5		ns
t_{PWHS}	VGAHS Pulsewidth	2			µs
t_{VS-HS}	VGAVS to VGAHS Delay	0			ns
t_S	Control Input Pulse Width, HIGH		50		ns
t_H	Control Input Pulse Width, LOW		50		ns
V_{RT}	Reference Voltage, Top	0.5	0.85	2.0	V
V_{IN}	Analog Input Range	0		V_{RT}	V
V_{REF}	Output Reference Voltage		1.25		V
I_{REF}	D/A Converter Reference Current		8.4		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		140		Ω
R_{OUT}	Total Output Load Resistance		50 (150//75)		Ω
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{IL}	Input Voltage, Logic LOW			0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C
T_C	Case Temperature, Still Air	30		105	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current, Operating	CVIDEN=H, SVIDEN=H		300		mA
I_{DDSV}	S-Video Active	CVIDEN=L, SVIDEN=H		280		mA
I_{DDCV}	Composite Video Active	CVIDEN=H, SVIDEN=L		240		mA
I_{DDS}	Standby	CVIDEN=L, SVIDEN=L		220		mA
I_{DDQ}	Power Supply Current, Power-Down	V_{DD} = Max, PWRDN\ = LOW		70		mA
V_{RO}	Voltage Reference Output			1.25		V
Z_{RO}	V_{REF} Output Impedance			750		Ω
C_{AI}	Input Capacitance, A/D	ADCLK = LOW		10		pF
		ADCLK = HIGH		10		pF
R_{IN}	Input Resistance		500	1000		KΩ
I_{CB}	Input Current, Analog				±15	µA
C_I	Digital Input Capacitance			5	10	pF
C_O	Digital Output Capacitance			10		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DS}	Sync Output Delay	VGA Sync to Sync Out		100		ns
t_{DOV}	Analog Output Delay	PXCK Out to Video Out			15	ns
t_R	D/A Output Current Risetime	10% to 90% of Full Scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of Full Scale		2		ns

Input System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
E_{LI}	A/D Integral Linearity Error, Independent	V_{RT} = 2.0V		±0.5	±1.3	LSB
E_{LD}	A/D Differential Linearity Error	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{AP}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	R_T - V_{IN} for most positive code transition	-20	45	80	mV
E_{OB}	Offset Voltage, Bottom	V_{IN} for most negative code transition	30	65	110	mV

Note: Values shown in Typ column are typical for $V_{DD} = V_{DDA} = +5V$ and $T_A = 25°C$.

Output System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	D/A Converter Resolution		10	10	10	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp		0.5		degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp		1.5		%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination			±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination			±1.0	%
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 µF, f = 1 KHz		0.5		%/ %V_{DD}

Notes:
1. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode".

Table 6. AIT1168 MQFP Package - Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AGND	21	DGND	41	NC	61	DGND
2	COMPOSITE	22	DGND	42	FIL	62	V_{DD}
3	R_{REF}	23	DGND	43	DGND / UV_SEL	63	GND_{PLL}
4	V_{REF}	24	I^2C_ADR	44	VSCOM	64	PLL_{LPF}
5	DGND	25	DGND	45	VGAVS	65	V_{DDPLL}
6	PHASE	26	VSOUT	46	VGAHS	66	AGND
7	V_{DD}	27	HSOUT	47	POS_R	67	CSYNC
8	DGND	28	DGND	48	POS_D	68	NC
9	V_{DD}	29	V_{DD}	49	AGND	69	$XTAL_1$
10	I^2C_SDA	30	DGND	50	B	70	$XTAL_2$
11	NC	31	DGND	51	V_{DDA}	71	RESET\
12	PXCK	32	DGND	52	V_{DDA}	72	PWRDN\ / I^2C_EN\
13	I^2C_SCL	33	V_{DD}	53	G	73	SVIDEN
14	V_{DD}	34	V_{DD}	54	AGND	74	CVIDEN
15	DGND	35	V_{DD}	55	V_{RT}	75	V_{DDA}
16	NC	36	DGND	56	V_{TOUT}	76	V_{DDA}
17	NC	37	DGND	57	V_{TIN}	77	C_{BYPR}
18	DGND	38	BLANK	58	AGND	78	CHROMA
19	DGND	39	NC	59	R	79	AGND
20	DGND	40	$TVSTD_0$	60	V_{DDA}	80	LUMA

Figure 2. AIT1168 80 Lead Metric Quad Flat Pack (MQFP) Outline

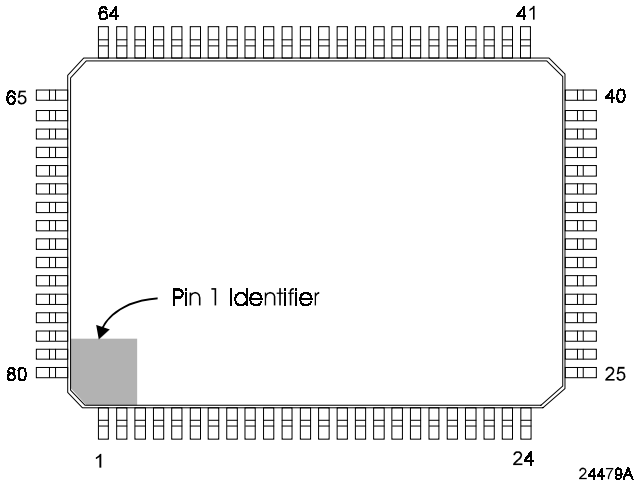

Figure 3. AIT1168 80-Lead Metric Quad Flat Pack (MQFP) Dimensions

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions D_1 and E_1 do not include mold protrusion. Allowable protrusion is 0.010 inch (0.245 mm)
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimensions ND, NE: number of terminals per package edge.
6. Controlling dimension: mm.

Dimensions

Millimeters (Inches)			
Sym	Min	Max	Notes
A		3.40(.134)	
A_1	0.15(.005)	0.35(.014)	
B	0.30(.012)	0.45(.018)	
D	23.90(.941) Basic		
D_1	20.00(.787) Basic		Note 2
E	17.90(.705) Basic		
E_1	14.00(.551) Basic		Note 2
e			0.80(.031) Basic
L	0.73(.029)	1.03(.041)	
N			80, Note 4
ND			24, Note 5
NE			16, Note 5

Ref. 90X00181

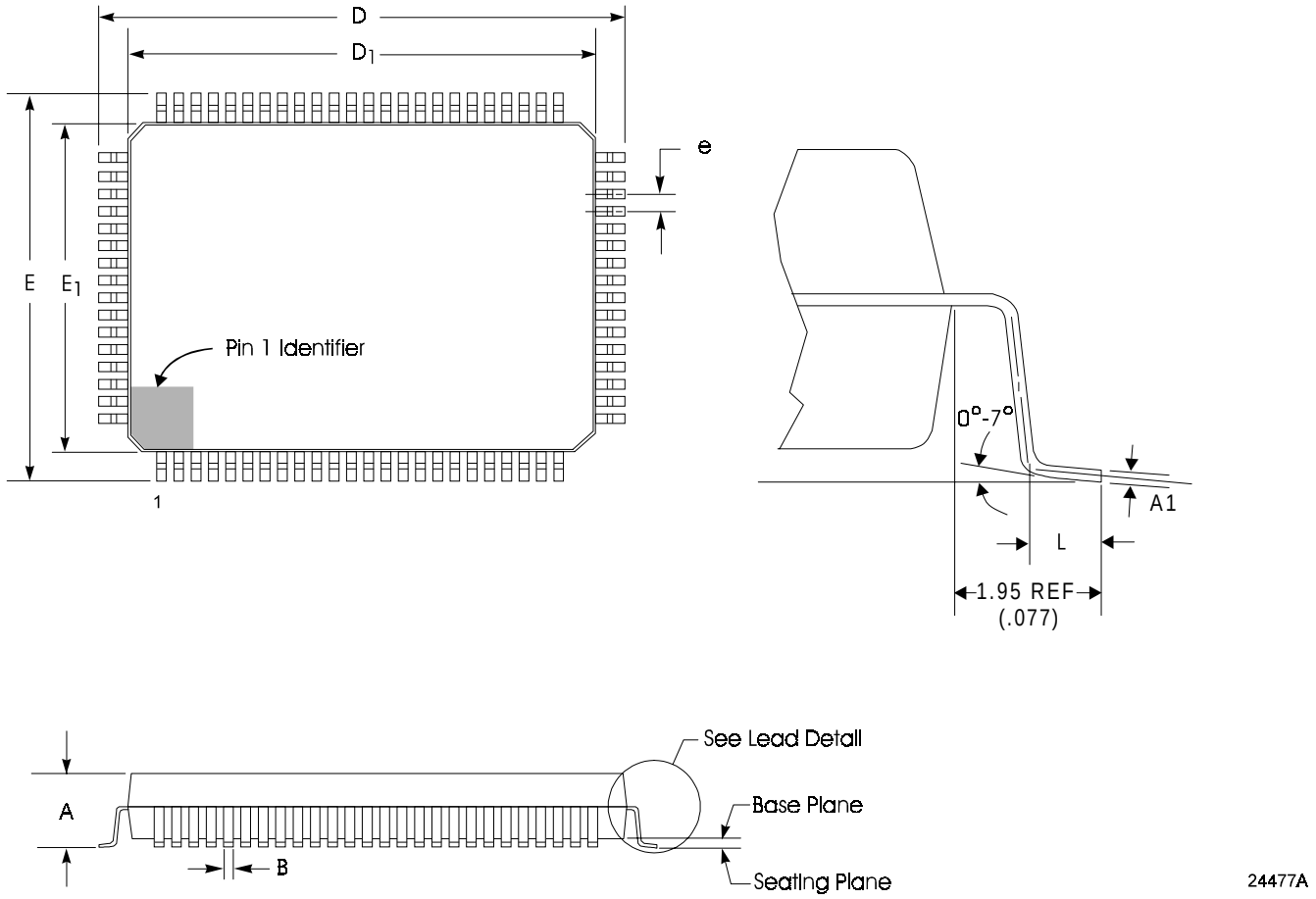

Table 7. IC Function Comparison

	AIT1168	AIT1108	Comment
Functions			
Power-Down	Yes	Yes	Power saving
Zoom	No	No	Master mode function, needs external memory
Blank	Yes	Yes	Blanks the TV output
Filter 3-2-1-Bar	Yes	Yes	switch between 3-line, 2-line, no-filter, and Color Bar
Color bar	Yes	Yes	Color bar display can be triggered by Filter pin
Slave/Master	Slave	Slave	Slaved timing to incoming VGA HSync
VSCOM	Yes	Yes	Software control using Sync
Freeze	No	No	Master mode only
Pos-Up	No*	No	Positioning controls. *Up is available only when 4-position control is set
Pos-Left	No*	No	Positioning controls. *Left is available only when 4-position control is set
Pos-Right	Yes	Yes	
Pos-Down	Yes	Yes	
SETUP			
Phase	Yes	Yes	A/D acquisition clock phase adjust
Ramtype	No	No	Memory select
2/4 pos	Yes	No	Selects between 2 or 4 button positioning control
Fastmem	No	No	Master mode function, require fast access memory
Blue	No	Yes	Choose between Black or Blue during blanking
TVstd [1:0]	auto detect	3-mode	AIT1168 auto-detects PAL/NTSC. TVSTD0 is used to select between NTSC or NTSC-EIA.
DPMS	No	Yes	Enables/Disables VESA DPMS power saving mode. DPMS in AIT1168 can no longer be disabled
I^2C Interface	Yes	No	
MISC.			
Csync	Yes	No	Composite sync output, SCART compatible
Narrow HS	Yes	No	To work with Notebook computer

Even Hor. lines	No	No	524 or 526 line/frame
HS/VS auto pulse reform	Yes	Yes	Auto-detects positive HS/VS, and change to -ve
S-Video Enable	Yes	Yes	Disables S-Video output to conserve power
Composite enable	Yes	Yes	
ANALOG			
Ext. PLL loop filter	Yes	Yes	Internally control only
DAC	10 150//75	9 75//75	AIT1168 use 150Ω//75Ω loading to save power
ADC	8	8	
Clock source	27Mhz	27Mhz	
VGA input mode	7 slave modes	3 slave modes	
640x480 Overscan NTSC	Yes	Yes	
640x480 Underscan NTSC	Yes	No	AIT1168 requires VGA timing change
640x480 Underscan PAL	Yes	Yes	Default PAL is underscan in 640x480
640x480 Overscan PAL	Yes	No	Horizontal only
800x600 Overscan NTSC	No	No	Converts 640x480 video area, selectable using pan control
800x600 Underscan NTSC	Yes	No	Requires VGA timing change
800x600 Overscan PAL	Yes	Yes	
800x600 Underscan PAL	Yes	No	Requires VGA timing change
MAC 640x480 @66 Hz NTSC/PAL	No	No	
NEC 640x400 NTSC/PAL	No	No	