

AIT1108E Video Signal Processor^(TM) (VSPPro)^(TM)

U. S. Patent S/N: 5526055

VGA to NTSC/PAL Converter

The AIT1108E accepts analog RGB and Syncs from a standard VGA source and converts it into broadcast-quality NTSC or PAL video signals. Simultaneous composite and S-Video outputs are provided, meeting all SMPTE-170M and CCIR-656 specifications. A fully-integrated digital *Flic-Free*^(TM) anti-flicker filter provides clear and stable video conversion.

The VSPPro requires an absolute minimum of external components. Precision timing is derived from a single 27 MHz crystal or clock reference.

All control is via package pins, and no additional microcontroller is required. Video and filtering modes may also be selected through software by programming the VSYNC timing. VESA Display Power Management Signaling (DPMS) is supported.

Available as AIT1108KMC in a 80-lead Thin MQFP and AIT1108ROC in a 84-lead PLCC.

Advance Information**

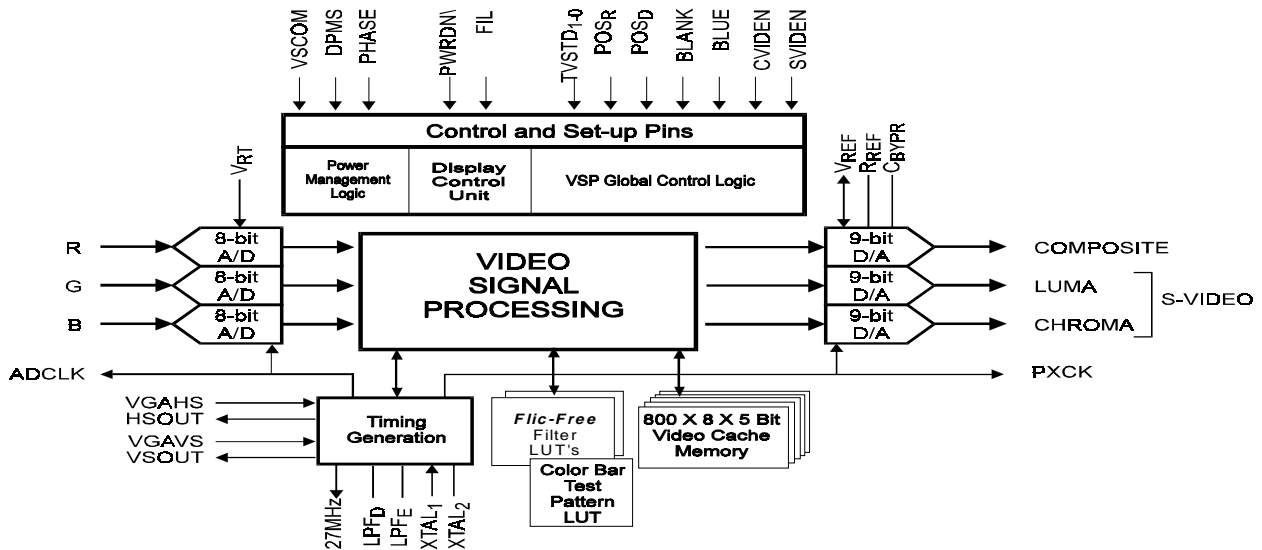
Feature

- ◆ Single-Chip Graphics-To-Video Processing
- ◆ Fully integrated with no external memory requirement
- ◆ No Microcontroller Needed
- ◆ 1:1 Aspect Ratio Conversion
- ◆ 3-Channel 8-Bit Input Digitizer
- ◆ Multiple Input Formats
640x480 50- And 60-Hz And 800x600 50-Hz
- ◆ 3-Channel 9-bit Output D/A Converters
- ◆ Multiple Output Standards
- NTSC, NTSC-EIA, PAL-B/G/H/I
- ◆ Composite And S-Video Output Formats
- ◆ Built-in Color Bars test pattern
- ◆ Blanks To Blue Or Black
- ◆ Single +5V Power Supply

Applications

- ◆ VGA to Video Converter Modules
- ◆ Computer Video Outputs for Multimedia PC
- ◆ Video Games
- ◆ Multimedia TV
- ◆ TV set-top box
- ◆ Video CD Player
- ◆ Network Computer
- ◆ Internet Appliance

Block Diagram



Functional Description

The AIT1108E is a single-chip VGA-to-Video converter, capable of producing broadcast-quality signals in all NTSC and PAL standards. The design provides all the active circuitry required to generate a television signal with outstanding, fully digital, image quality in a stand-alone application.

The input VGA signal must be set at 2X the frame and line rate of the output TV video standard within $\pm 2\%$. This is the normal operating condition for the standard 640x480 VGA mode converting to a 30Hz video frame rates (NTSC, PAL-M). The VGA graphics controller will have to be reprogrammed to a 50Hz frame rate to support conversion to other PAL standards with a 25Hz video frame rates.

The AIT1108E is ideal for portable scan converter applications and for integration into notebook and palmtop computers, video games, Internet appliances, network computer, TVs, and set top boxes.

Input Section

The analog VGA signal is digitized by three 8-bit A/D converters, operating at rates of up to 36 Msp. The high input impedance and low noise of the A/D section imposes minimal load and distortion on the VGA signals.

The standard signal range from the VGA's output should be between 0.0V to 0.85V, and should match up with the A/D's reference voltage, V_{RT} . V_{RT} may be supplied by the on-chip voltage follower V_{TOUT} with input V_{TIN} .

Clock Processor

All operating clocks are derived from VGAHS, the horizontal sync signal from the VGA controller. An internal phase-locked-loop synchronizes data sampling clock with the VGA mode in use, ensuring accurate sampling of the graphics signal. This clock is available on pin ADCLK for reference.

A second PLL generates the digital encoder's clock, which can be found on pin PXCK. A stable timebase reference is produced by a 27 MHz crystal or, alternatively, by an externally generated TTL clock applied to pin XTAL₁. Loop filters for the two clock PLLs must be connected to LPF_D and LPF_E.

Vertical timing information is derived from VGAVS, the vertical sync signal from the VGA controller. This synchronizes the video encoder with the incoming signal. HSYNC and VSYNC may be of either polarity: the AIT1108E automatically determines and accommodates any combination.

Operational commands may be conveyed from the PC to the chip over the VGAHS and VGAVS signals. The chip detects and responds to the VESA DPMS controls, blanking the screen when commanded to Stand-by or Suspend mode, and going to Power-Down mode when commanded Off. DPMS response may be disabled through the DPMS pin.

Flicker filter mode and video standard may be set from the PC by controlling the length of VGAVS. This control may be disabled via the VSCOM pin.

Flicker Filter

The *Flic-Free*^(TM) anti-flicker filter is an adaptive flicker filter derived from AITech's expertise in providing high quality scan converters. It provides the user with three options in the filter level. A single toggle pin (FIL) selects among High Filter, Medium Filter, and No Filter modes. A fourth state, Color Bars, provides a useful video setup and test signal, as well as a reference point for filter selection.

Video Encoder

The Video Encoder Section is a high-performance multistandard encoder for Settop, Desktop, and Broadcast Video applications. The all-digital circuit employs the latest technology in Digital Signal Processing to ensure solid, no-drift performance with no tuning in manufacturing.

The television standard to be produced is selected via the TVSTD₁₋₀ pins, unless VSCOM is enabled. The image may be moved right, left, up, and down by toggling the POS_R and POS_D pins. The video may be blanked with the BLANK pin, and the blank screen may be set to black or blue via the BLUE pin.

Three 9-bit D/A converters produce clean, noise-free video signals that can drive 75 Ω or 37.5 Ω (a double-terminated 75 Ω line) loads. Digital oversampling of the video datastream minimizes distortion and permits the use of very low-cost R-C output filters. Output current is established by V_{REF} and a resistor connected between R_{REF} and ground. An internal 1.235 volt reference is buffered from V_{REF} by a resistor, so V_{REF} may be overridden by an external voltage. Output current may be calibrated by resistor selection or setting a potentiometer attached to R_{REF}. A bypass capacitor must be connected to C_{BYPR} to minimize noise.

The Composite and S-Video D/As can be independently enabled (via CVIDEN and SVIDEN pins) to minimize power consumption.

Control Processor

The control processor coordinates all functions of the chip. The AIT1108E can be completely controlled by a combination of push buttons and switches. All toggle (push button) functions have Schmitt trigger inputs. Any features not desired in a particular implementation may be hard-wired.

Analog Reference

An on-board reference circuit is provided to feed both the input section and the video encoder. The reference voltage is set by a single resistor, and may be calibrated through resistor selection or with a pot. The Encoder and A/Ds are driven by the reference circuit through resistors, but they may be independently overdriven by external reference voltages. Bypass capacitors should be applied to C_{BYPA} and C_{BYPR}.

Package Interconnections

| Signal Type | Name | Function | Type/ Value | Package/Pin | |
|------------------|----------------------|---|-------------------|-------------|------------|
| | | | | MQFP | PLCC |
| Clock | ADCLK | A/D Converter Clock Output | TTL | 13 | 22 |
| | LPF _D | A/D PLL Loop Filter Connection | - | 64 | 77 |
| | PXCK | Encoder Clock Output | TTL | 12 | 21 |
| | LPF _E | Encoder PLL Loop Filter Connection | - | 67 | 80 |
| | XTAL ₁₋₂ | Subcarrier Reference Crystal/Clock | - | 70,69 | 83, 82 |
| | 27MHZ | Subcarrier Reference Clock Output | CMOS | 11 | 20 |
| | A0 | External PXCK PLL Select | TTL | 32 | 43 |
| | A1 | External ADCLK PLL Select | TTL | 31 | 42 |
| | ADIVN | Internal ADCLK divided by N output | TTL | 16 | 25 |
| | PDIVM | Internal PXCK divided by M output | TTL | 17 | 26 |
| Global Controls | TVSTD ₁₋₀ | Video Output Standard Select | CMOS _P | 39, 40 | 50, 51 |
| | PAL800 | Resolution select for PAL. | CMOS _P | 41 | 52 |
| | DPMS | Display Power Management Signaling Enable | CMOS _P | 43 | 54 |
| | FIL | Flicker Filter Mode Select | TTL _S | 42 | 53 |
| | VSCOM | Vertical Sync Communications Enable | CMOS _P | 44 | 55 |
| | PWRDN | Power-Down Control | CMOS _P | 72 | 1 |
| | RESET | Reset | CMOS _P | 71 | 84 |
| | PHASE | Sampling Phase Control | CMOS _P | 6 | 15 |
| Encoder Controls | CVIDEN | Composite Video D/A Power Enable | CMOS _P | 74 | 3 |
| | SVIDEN | S-Video D/A Power Enable | CMOS _P | 73 | 2 |
| | BLANK | Blank Screen Generator | CMOS _P | 38 | 49 |
| | BLUE | Blank Screen Color Selector | CMOS _P | 37 | 48 |
| | POS _{R, D} | TV Image Position Controls | TTL _S | 47, 48 | 58, 59 |
| Video Inputs | R, G, B | Analog RGB inputs | 0.85 V p-p | 59, 53, 50 | 70, 64, 61 |
| | V _{TIN} | A/D Converter Reference Input, Buffered | +0.85V | 57 | 68 |
| | V _{TOUT} | A/D Converter Reference Output, Buffered | +0.85V | 56 | 67 |
| | V _{RT} | A/D Converter Reference Input, Unbuffered | +0.85 V | 55 | 66 |
| | VGAHS | VGA Horizontal Sync | TTL _S | 46 | 57 |
| | VGAVS | VGA Vertical Sync | TTL _S | 45 | 56 |
| Video | COMPOSITE | NTSC/PAL Video Output | 1 V p-p | 2 | 11 |

| Signal Type | Name | Function | Type/ Value | Package/Pin | |
|-------------------|---------------------|---------------------------------|----------------|--|--|
| | | | | MQFP | PLCC |
| Outputs | LUMA | Luminance-only Video | 1 V p-p | 80 | 9 |
| | CHROMA | Chrominance-only Video | 1 V p-p | 78 | 7 |
| | HSOUT | Buffered VGAHS Output | TTL | 27 | 38 |
| | VSOUT | Buffered VGAVS Output | TTL | 26 | 37 |
| Encoder Reference | V _{REF} | Voltage Reference Input/Output | +1.23 V | 4 | 13 |
| | C _{BYPR} | Reference Bypass Capacitor | 0.1 μF | 77 | 6 |
| | R _{REF} | Current-setting Resistor | 392Ω | 3 | 12 |
| Power | V _{DD} | Digital Power Supply | +5.0 V | 7, 9, 14, 29, 33, 34, 35, 62, | 16, 18, 23, 40, 44, 45, 46, 73 |
| | V _{DDA} | Analog Power Supply | +5.0 V | 51, 52, 60, 75, 76 | 4, 5, 62, 63, 71 |
| | V _{DDPLLD} | A/D Phase Locked Loop Power | +5.0 V | 65 | 78 |
| | V _{DDPLLE} | Encoder Phase Locked Loop Power | +5.0 V | 68 | 81 |
| | DGND | Digital Ground | 0.0 V | 5, 8, 10, 15, 18, 19, 20, 21, 22, 23, 24, 25, 28, 30, 36, 61 | 14, 17, 19, 24, 27, 28, 29, 30, 31, 34, 35, 36, 39, 41, 47, 72 |
| | AGND | Analog Ground | 0.0 V | 1, 49, 54, 58, 63, 66, 79 | 8, 10, 60, 65, 69, 76, 79 |
| No Connect | DNC | Do Not Connect | | | 32, 33, 74, 75 |

CMOS_P = CMOS with light pull-up

TTL_S = TTL with Schmitt Trigger

Signal Definitions

Clock Generators

| | | | |
|---------------------|---|-------|---|
| ADCLK | A/D converter clock output generated by an internal phase-locked loop slaved to VGAHS. ADCK becomes an input when A0 is selected. | A1 | for generating PXCK. Select between internal or external PLL for generating ADCLK. |
| LPF _D | A/D clock PLL Loop Filter Node. An external RC network is connected here. | ADIVN | Internal ADCLK divided by N output. Can be used to feed the external PLL |
| PXCK | Line-locked encoder clock output generated by an internal phase-locked loop slaved to VGAHS. PXCK becomes an input when A1 is selected. | PDIVM | Internal PXCK divided by M output. Can be used to feed the external PLL. |
| LPF _E | Encoder clock PLL Loop Filter Node. An external RC network is connected here. | | |
| XTAL ₁₋₂ | Subcarrier reference crystal/clock. Connection terminals for an external 27 MHz crystal. Alternatively, the XTAL ₁ pin may be used as an input from an external oscillator or clock. Subcarrier frequency accuracy is based on this clock. | | |
| 27MHz | Subcarrier Reference Clock Output. Buffered TTL output from 27MHz crystal oscillator/reference clock. | | |
| A0 | Selects between internal or external PLL | | |

Global Controls

| | |
|----------------------|---|
| TVSTD ₁₋₀ | Video output standard select. Preprogrammed into the VSPro are timing, subcarrier frequency and phase parameters corresponding to worldwide NTSC and PAL standards. TVSTD ₁₋₀ select one of four sets of parameters to set up the encoder. Frame rate of the graphics source must be twice the frame rate of the selected video standard. |
| PAL800 | Resolution select for PAL. Sets number of samples per VGA line. |
| DPMS | Display Power Management Signaling enable. When HIGH, the operational state of the VSPro is controlled by the pulse activity on VGAHS and VGAVS. When LOW, the state of the VSPro is controlled only by input pins. |
| FIL | Flicker filter mode select. The adaptive flicker reduction filter may be configured for HIGH filtering, MEDIUM filtering, or NO filtering by pulsing this input HIGH. FIL defaults to HIGH-filter mode upon power-up. If VSCOM is HIGH, the filter mode will be selected by the pulsewidth of VGAVS, and FIL will be ignored. The FIL input is a Schmitt trigger. |
| VSCOM | Vertical sync communications enable. When HIGH, vertical sync pulse width (VGAVS) will control the filter mode, and FIL will be ignored. |
| PWRDN \setminus | Power-down control. When HIGH, the VSPro is fully operational and enabled. When LOW, the VSPro is configured for minimum power consumption. D/A converters and clocks are disabled. Previously established set-up conditions are retained and remain in effect when PWRDN \setminus goes HIGH. |
| VGAHS | Horizontal sync input from VGA input. Incoming VGA sync may be of either polarity (active LOW or active HIGH). VGAHS frequency must be within $\pm 2\%$ of the nominal specified value. The VGAHS pin has a light pull-up and a Schmitt trigger. |
| HSOUT | Horizontal Sync Output. Buffered output that follows VGAHS. |
| VGAVS | Vertical sync input from VGA input. Incoming VGA sync may be of either polarity (active LOW or active HIGH). The VGAVS pin has a light pull-up and a Schmitt trigger. |
| VSOUT | Vertical Sync Output. Buffered output that follows VGAVS. |
| PHASE | Sampling phase control. Shifts the A/D |

sampling phase by 180°.

RESET \setminus Initializes internal registers

Encoder Controls

| | |
|--------------------|---|
| CVIDEN | Composite Video D/A Power Enable. When HIGH, the COMPOSITE D/A converter is enabled. When LOW it is disabled to save power. |
| SVIDEN | S-Video D/A Power Enable. When HIGH, the CHROMA and LUMA D/A converters are enabled. When LOW, they are disabled to save power. |
| BLANK | Blank screen generator. When HIGH, the color selected by BLUE is displayed on the screen. When LOW, incoming video from the internal FIFO is encoded. |
| BLUE | Blank screen color selector. When HIGH, the screen will be blanked to blue when BLANK is HIGH. When LOW, the screen will be blanked to black when BLANK is HIGH. |
| POS _{D,R} | TV image position controls. Position controls shift the VGA image horizontally or vertically, revealing portions that are found near the edges or in the overscan areas. Default power-up position is the midpoint of the adjustment range. POS _{D,R} inputs are Schmitt triggers. |

A/D Converter Interface

| | |
|-------------------|---|
| R, G, B | Analog red, blue and green inputs to the A/D converters from incoming VGA signals. Nominal voltage range is 0.0 to +0.85 Volts. |
| V _{RT} | Unbuffered Top Reference Voltage for the three A/D Converters. Supplies current to A/D converters' reference resistors. May be driven from V _{TOUT} . Voltage range is 0.5 to 2.0 volts. |
| V _{TIN} | Input to Top Reference Voltage Buffer, a voltage follower may be connected to V _{RT} . |
| V _{TOUT} | Top Reference Voltage Buffer Output that may be connected to V _{RT} to supply current to A/D converter reference resistors. In power down mode, V _{TOUT} drops to zero. |

Video Output

| | |
|------------|---|
| COM-POSITE | Composite Video. NTSC/PAL baseband composite output can drive 1 Volt p-p video into a 37.5 Ohm load. This composite signal contains sync, subcarrier and active video information to drive monitors, projectors, VCRs, and other video devices. |
| LUMA | Luminance-only video. This analog monochrome video output can drive 1 Volt p-p video into a 37.5 Ohm load. The luminance signal contains all sync and active |

video information necessary. to drive black-and-white video devices.
CHROMA Chrominance-only video. This analog output can drive a 37.5 Ohm load. **CHROMA**

Voltage Reference

- V_{REF}** Output of an internal 1.23 Volt band-gap voltage reference. If unconnected, except for a 0.1µF capacitor to ground for noise decoupling, the internal reference will be used for the three D/A converters. An externally generated voltage reference of +1.2 Volts applied to the V_{REF} pin will override the internal voltage reference and become the new reference for the D/A converters.
- R_{REF}** A resistor of 392Ω is connected between the R_{REF} terminal and ground to establish the reference current for the three internal D/A converters. The value of this resistor determines the full-scale output current (and therefore the peak video level) of the D/A converters.
- C_{BYPR}** An external 0.1µF capacitor should be connected between C_{BYPR} and V_{DDA} to reduce noise on the internal reference circuitry.

signal, when combined with LUMA comprises an S-Video signal suitable for driving monitors, projectors, VCRs, and other S-Video devices.

Power and Ground

- V_{DD}** Digital power. Supplies +5V power to internal digital circuits.
- V_{DDA}** Analog power. Supplies +5V power to internal analog circuits. V_{DD} and V_{DDA} must originate from the same source.
- V_{DDPLL}** A/D phase-locked loop +5V power. V_{DDPLLE} and V_{DD} must originate from the same source.
- V_{DDPLe}** Encoder phase-locked loop +5V power. V_{DDPLL} and V_{DD} must originate from the same source
- DGND** Digital ground. Ground point for internal digital circuits.
- AGND** Analog ground. Ground point for internal analog circuits. DGND and AGND should be connected to the same ground plane.

Clocks

A/D Clock (ADCLK)

ADCLK is the buffered analog-to-digital converter clock output which is derived from incoming VGA horizontal sync (VGAHS) by a phase-lock loop (PLL).

A/D Clock frequency is set by the PLL divide-by-N counter where N is the number of A/D samples between the horizontal sync pulses in each VGA line.

Pre-programmed values selected by the TVSTD₁₋₀ and PAL800 control inputs set N and the clock frequency as shown in *Table 1*.

Table 1. VGA A/D Clock

| Television Standard | TVSTD ₁₋₀ | PAL800 | ADCLK Freq. (MHz) | A/D N |
|---------------------|----------------------|--------|-------------------|-------|
| NTSC | 0x | 0 | 25.175 | 800 |
| PAL640 | 10 | 0 | 25.250 | 808 |
| PAL800 | 10 | 1 | 36.000 | 1152 |

The recommended configuration of the loop filter that should be connected to the LPF_D pin will be a 39K resistor in series with a 0.1uF capacitor and these two components are parallel to a 680pF capacitor to ground.

Pixel Clock (PXCK)

PXCK is the buffered video encoder clock output which is derived from the incoming VGA HSYNC signal by a second phase-lock loop. The recommended loop filter, to be connected to LPFE, is identical to the LPFD loop filter.

Clock frequency is set by the PLL divide-by-M counter. M is the number of encoder samples between horizontal sync pulses and, because of 2X oversampling, is twice the TV square pixel rate. Active pixels in each VGA line are digitized according to pre-programmed values selected by the TVSTD₁₋₀ and PAL800 control inputs. *Table 2* shows the video output timing.

Table 2. NTSC and PAL Pixel Clocks

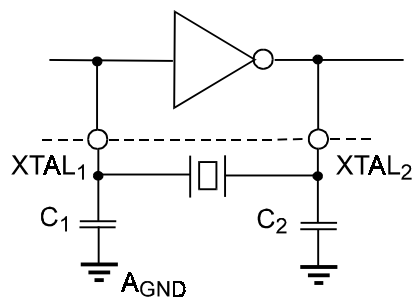
| Television Standard | Line Rate (kHz) | Pixel Rate (MHz) | PLL M |
|---------------------|-----------------|------------------|-------|
| NTSC | 15.734 | 24.540 | 780 |
| PAL | 15.625 | 29.500 | 944 |

Using the A0 and A1 pins, either one or both of the internal PLL's can be overwritten.

Reference Clock

Accuracy of the PAL/NTSC subcarrier depends on the 27 MHz reference signal applied to the XTAL₁. This signal may be derived from a clock connected directly to the XTAL₁ pin or a crystal and capacitors connected across XTAL₁₋₂ as shown in *Figure 1*.

Figure 1. Crystal Oscillator Circuit



Capacitors C₁ and C₂ must be adjusted to trim the frequency within ±20 ppm. C₁ and C₂ have the same value, with series capacitance equal to the load recommended for the crystal. Typical crystal parameters are ±50 ppm accuracy with a 20 pF load and ±80 ppm pull.

Digitizing

A/D Reference

An on-chip voltage follower is designed to supply current to the ADC reference V_{RT} from V_{TOUT}. A stable voltage source greater than the input peak amplitude should be connected to V_{TIN}. V_{RT} should be equal or smaller than the maximum RGB video input signal.

Input Signal Conditioning

ADC performance can be optimized by driving the RGB video inputs with either a 75 ohm or a low impedance source.

Input Format Selection

One of four input VGA formats can be accepted by setting the TVSTD₁₋₀ and PAL800 inputs as shown in *Table 3*. Each VGA input option corresponds to a VGA active video area, frame rate and line rate with a corresponding TV output format.

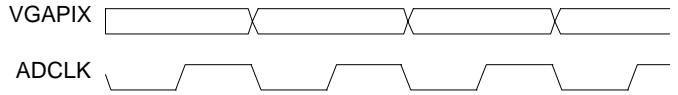
Table 3. VGA Input Formats

| TVSTD ₁₋₀ | PAL800 | H x V Input Pixels | Frame Rate (Hz) | Line Rate (kHz) |
|----------------------|--------|--------------------|-----------------|-----------------|
| 0x | 0 | 640 x 480 | 59.94 | 31.469 |
| 10 | 0 | 640 x 480 | 50 | 31.250 |
| 10 | 1 | 800 x 600 | 50 | 31.250 |
| 11 | 0 | 640 x 480 | 59.94 | 31.469 |

Sampling Phase Control

Conversion can be optimized by using the PHASE control to set the sampling points of the A/D clock to lie between the VGA pixel transitions. *Figure 2* shows optimum sampling of VGA pixels on the rising edge of the ADCLK signal.

Figure 2. Sampling of VGA Pixels



PHASE selects the conversion edge of the ADCLK. If PHASE = LOW, the rising edge is selected. If PHASE = HIGH, the falling edge is selected.

Processing

Flicker Filter

Annoying artifacts can be eliminated by selecting one of three filter modes, which trade-off vertical resolution against flicker. Without the filter, one contrasting VGA line may be encoded into one field of the TV video, which will flicker at 30 Hz with NTSC and 25 Hz with PAL. As shown in *Table 4*, if VSCOM = LOW, pulsing the FIL pin indexes the VSPro through a loop of three filter modes and a color bar pattern.

Table 4. FIL Filter Mode Select Sequence

| FIL | Filter Mode |
|-----|----------------|
| ↓ | HIGH (default) |
| ↓ ↑ | MEDIUM |
| ↓ | No filter |
| | Color bars |

Video Encoder

D/A Reference

Peak D/A converter current for the video outputs is set by a resistor connected to R_{REF}. For a 37.5 ohm load, the correct value of R_{REF} is 392 ohm. To trim the video output level, R_{REF} can be replaced with a potentiometer.

Television Standard Selection

NTSC and PAL standards are preprogrammed with preset horizontal and vertical timing, subcarrier frequency, and chrominance phase. Frame rate of the VGA source must match the field rate of the selected video standard. Depending upon the status of the Vertical Sync Communications (VSCOM) pin, the video output format may be selected by either the TVSTD₁₋₀ pins or by VSCOM codes.

Table 5 shows how the TVSTD_{1,0} pins select the TV output format with VSCOM = LOW.

Table 5. TVSTD Control When Under Manual Control (VSCOM=0)

| TVSTD ₁₋₀ | Television Standard | Video Field Rate |
|----------------------|---------------------|------------------|
| 00 | NTSC-EIA | 60 Hz |
| 01 | NTSC | 60 Hz |
| 10 | PAL/B, G, I | 50 Hz |
| 11 | Reserved | Reserved |

If VSCOM = HIGH, Vertical Sync Communications are enabled. VSCOM is described under the Vertical Sync Command section below.

Image Positioning

The POS_D and POS_R position controls change the encoder timing relative to incoming PC video, shifting the viewed image either horizontally or vertically to reveal portions of the image located near the edges or in the overscan areas. At power-up, the default position is the midpoint of the adjustment range.

Each POS_D HIGH pulse moves the TV window down eight lines. At the lowest position (-64 lines) the direction reverses and the pulses move the image up in 8-line

increments to the highest position (+64 lines). At this point the direction again reverses and the next sixteen pulses move the image down to the lowest position.

Each POS_R HIGH pulse moves the TV window eight pixels to the right. At the maximum right position (+64 pixels) the direction reverses and the next sixteen pulses move the window left to the maximum left position (-64 pixels). Direction again reverses and the next sixteen pulse move the image right.

Without a RESET, POS_{D,R} controls will loop, causing the window to move down/up, right/left.

Blank and Blue

TV video can set to active (converted VGA source), blank or blue by the BLANK and BLUE inputs.

Table 6. Video Output for BLANK and BLUE inputs

| BLANK | BLUE | Video |
|-------|------|-------|
| L | X | Video |
| H | L | Black |
| H | H | Blue |

Power Management

D/A Power Control

Table 7 shows how the Composite and S-video outputs are enabled by the CVIDEN and SVIDEN controls. With DPMS = LOW, if VGA horizontal and vertical sync signals are missing, then both video outputs are set to blue.

Powerdown Mode

PWRDN\ eliminates current drain by the D/A converter, V_{TOUT} voltage follower and clock outputs. With PWRDN\ = HIGH, all outputs are enabled. If PWRDN\ = LOW, all outputs are disabled including the ADCLK, PXCK, V_{TOUT} and the D/A converters.

Table 7. Video Output Control

| CVIDEN | SVIDEN | VGAHS & VGAVS | Composite Video | S-Video |
|--------|--------|---------------|-----------------|---------|
| H | X | YES | Active | X |
| X | H | YES | X | Active |
| L | L | X | Blank | Blank |
| X | X | NO | Blue | Blue |

Software Control

Display Power Management Signaling (DPMS)

Display Power Management is compliant with VESA DPMS Proposal 1.0. With DPMS = HIGH, the operational state of the VSP_{ro} is controlled by the pulse activity on VGAHS and VGAVS.

Table 8. shows how the VSP_{ro} responds. “No Pulses” on VSYNC or HSYNC is declared on the second missing VSYNC or HSYNC pulse. Following an OFF state,

detection of VGAHS and/or VGAVS restores either the Suspend, Standby, or On state.

If DPMS = LOW, the display will be blue if either or both VGHS or VGAVS are inactive.

Regardless of the state of DPMS, absence of VGAHS and/or VGAVS pulses will cause the VSP_{ro} processor to sleep. However, with DPMS=HIGH, in the Off state. the A/Ds, D/As, and clocks are also set to sleep.

Table 8. Display Power Management Signaling (DPMS) States

| State | VGAHS | VGAVS | VSP _{ro} State |
|----------|-----------|-----------|--|
| On | Pulses | Pulses | On, video active |
| Stand-by | No Pulses | Pulses | Stand-by, screen blanked (color set by BLUE) |
| Suspend | Pulses | No Pulses | Stand-by, screen blanked (color set by BLUE) |
| Off | No Pulses | No Pulses | Off, (equivalent to “PWRDN”). |

Vertical Sync Communications (VSCOM)

VSCOM is a unique feature incorporated into the VSP_{ro}. With VSCOM = HIGH, the VSP_{ro} interprets commands that are encoded within the VGA vertical sync period. With VSCOM, both the TV Standard and the Flicker

Filter may be selected by commands from the PC sourcing the VGA signal.

During the vertical sync period, the number of horizontal sync pulses is counted.

Table 9 shows how the selected Television Standard changes with the code set into the TVSTD₁₋₀ inputs and

the number of horizontal syncs per vertical sync interval.

Table 9. TVSTD Control When Under Software Control (VSCOM=1)

| TVSTD ₁₋₀ | Hsyncs per Vsync Interval | Television Standard | VGA Frame Rate |
|----------------------|---------------------------|-----------------------------|----------------|
| XX | 10,11,12 | PAL 800 (BGI) | 50 Hz |
| X0 | 6,7,9 | PAL 640 (BGI) | 50 Hz |
| 01 | 6,7,9 | (reserved) | |
| 11 | 6,7,9 | (reserved) | |
| 0X | 1-5,8,14,15 | NTSC-EIA | 60 Hz |
| 10 | 1-5,8,14,15 | NTSC | 60 Hz |
| 11 | 1-5,8,14,15 | (reserved) | |
| XX | 0,13 | Blank (with prior standard) | 50/60 Hz |

Table 10 shows how the Filter Mode is selected with VSCOM. Notice that if one standard, such as PAL800 is selected, then counts of 10, 11 and 12 enable selection of three filter modes.

Table 10. VSCOM Filter Command Interpretation (VSCOM=1)

| HSYNCS per VSYNC Interval | Filter Mode |
|---------------------------|-------------------------|
| 5, 9, 12 | No Filter |
| 4, 7, 11 | 2-line filter |
| 1, 2, 3, 6, 8, 10, 14, 15 | 3-line filter |
| 0, 13 | Blank (with prior mode) |

Video Formats

Incoming VGA Formats

Table 11 and Table 12 show the VGA Video input formats expected by the VSPPro.

Table 11. VGA Horizontal timing parameters

| Television Standard | TVSTD ₁₋₀ | PAL800 | Line Rate (kHz) | Front Porch (pixels) | Horiz Sync (pixels) | Back Porch (pixels) | Active Video (pixels) |
|---------------------|----------------------|--------|-----------------|----------------------|---------------------|---------------------|-----------------------|
| NTSC(-EIA) | 0x | x | 31.469 | 18 | 96 | 46 | 640 |
| PAL/B, G, I | 10 | 0 | 31.250 | 18 | 96 | 54 | 640 |
| PAL/B, G, I | 10 | 1 | 31.250 | 98 | 96 | 158 | 800 |

Table 12. VGA Vertical timing parameters

| Television Standard | TVSTD ₁₋₀ | PAL800 | Frame Rate (Hz) | Line Rate (kHz) | Full Frame (lines) | Front Porch (lines) | Vert. Sync (lines) | Vsync + Back Porch (lines) | Active Video (lines) |
|---------------------|----------------------|--------|-----------------|-----------------|--------------------|---------------------|--------------------|----------------------------|----------------------|
| NTSC(-EIA) | 0x | x | 59.94 | 31.469 | 525 | 13 | 2-16 | 32 | 480 |
| PAL/B, G, I | 10 | 0 | 50 | 31.250 | 625 | 61 | 2-16 | 84 | 480 |
| PAL/B, G, I | 10 | 1 | 50 | 31.250 | 625 | 1 | 2-16 | 24 | 600 |

Outgoing TV Formats

Table 14 and Table 15 show the Horizontal and Vertical Timing for the NTSC and PAL formats selected by the TVSTD1-0 inputs.

Table 13 shows the four different TV formats that may be selected as outputs.

Table 14 and Table 15 show the Horizontal and Vertical Timing for the NTSC and PAL formats selected by the TVSTD₁₋₀ inputs.

Table 13. TVSTD Control When Under Manual Control (VSCOM=0)

| TVSTD ₁₋₀ | Television Standard | Field Rate |
|----------------------|---------------------|------------|
| 00 | NTSC-EIA | 60 Hz |
| 01 | NTSC | 60 Hz |
| 10 | PAL/B, G, I | 50 Hz |
| 11 | Reserved | |

Table 14. NTSC and PAL horizontal timing

| Television Standard | Field Rate (Hz) | Lines per frame | Line Rate (kHz) | Sq pix Rate (MHz) | f _{sc} Freq. (MHz) | Front Porch pixels | Horiz Sync pixels | Back Porch pixels | Active Video pixels | Line H pixels |
|---------------------|-----------------|-----------------|-----------------|-------------------|-----------------------------|--------------------|-------------------|-------------------|---------------------|---------------|
| NTSC | 59.94 | 525 | 15.734 | 12.273 | 3.579 | 18 | 58 | 58 | 646 | 780 |
| PAL | 50.00 | 625 | 15.625 | 14.750 | 4.433 | 18 | 70 | 82 | 774 | 944 |

Table 15. NTSC and PAL vertical timing

| TV Std | Field Rate (Hz) | Lines per frame | Line Rate (kHz) | Front Porch (lines) | Vertical Sync (lines) | Back Porch (lines) | Active Video (lines) |
|--------|-----------------|-----------------|-----------------|---------------------|-----------------------|--------------------|----------------------|
| NTSC | 59.94 | 525 | 15.734 | 3-3.5 | 3 | 14-14.5 | 242.5 |
| PAL | 50.00 | 625 | 15.625 | 2.5 | 2.5 | 21 | 286.5 |

External Phase Lock Loops Selection

Using the A1 and A0 set-up pins, external PLL's could be used. Table 16 shows the different options. ADIVN and PDIVM provides the divide by N and divide by M

value for the A/D clock and PXCLK, respectively, to be used to program the dividers of the external PLL's. When using external PLL's, the ADCLK and PXCK pin switches from output to input.

Table 16. External PLL's select

| A1 | A0 | PLLA (A/D) | PLL (PXCK) | ADIVN | PDIVM | ADCLK | PXCK |
|----|----|------------|------------|-------|-------|--------|--------|
| 0 | 0 | Internal | Internal | Hi-Z | Hi-Z | Output | Output |
| 0 | 1 | Internal | External | 1/N | 1/M | Output | Input |
| 1 | 0 | External | Internal | 1/N | 1/M | Input | Output |
| 1 | 1 | External | External | 1/N | 1/M | Input | Input |

Absolute Maximum Ratings (beyond which the device may be damaged)¹

| | |
|--|--|
| Power Supply Voltages | |
| V _{D_{DDA}} (Measured to AGND) | -0.5 to +7.0V |
| V _{D_{DD}} (Measured to DGND) | -0.5 to +7.0V |
| V _{D_{DDA}} (Measured to VDD) | -0.5 to +0.5V |
| A _{GND} (Measured to DGND) | -0.5 to +0.5V |
| Digital Inputs | |
| Applied Voltage (Measured to DGND) ² | -0.5 to V _{D_{DD}} +0.5V |
| Forced current ^{3,4} | -10.0 to +10.0 mA |
| Analog Inputs | |
| Applied Voltage (Measured to AGND) ² | -0.5 to V _{D_{DDA}} +0.5V |
| Forced current ^{3,4} | -10.0 to +10.0 mA |
| Outputs | |
| Applied voltage (Measured to DGND) ² | -0.5 to V _{D_{DD}} + 0.5V |
| Forced current ^{3,4} | -6.0 to +6.0 mA |
| Short circuit duration (single output in HIGH state to ground) | 1 second |
| Temperature | |
| Operating, ambient | 0 to 70°C |
| junction | +150°C |
| case | +140°C |
| Storage | -20 to +70°C |
| Electrostatic Discharge ⁵ | ±150 V |

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

| Parameter | | Min | Nom | Max | Units |
|--------------------|--|-----------|--------|-----------------|-------|
| V _{DD} | Digital Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V _{DDA} | Analog Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| A _{GND} | Analog Ground (Measured to D _{GND}) | -0.1 | 0 | 0.1 | V |
| F _{xtal} | Crystal/Reference Clock Frequency | 26.998650 | 27 | 27.001350 | MHz |
| f _{XTOL} | Crystal/Reference Clock Frequency Tolerance | 0 | ±300 | ±1350 | Hz |
| f _H | VGAHS Frequency | | | | |
| | 59.94 Hz Modes | 30.840 | 31.469 | 32.100 | KHz |
| | 50Hz Modes | 30.630 | 31.250 | 31.880 | KHz |
| N _H | Lines per VGA field | | | | |
| | 59.94 Hz Modes | | 525 | | |
| | 50Hz Modes | | 625 | | |
| | Tolerance | | | ±0 | |
| t _{PWH} | Reference Clock Pulse Width, HIGH | | 18.5 | | ns |
| t _{PWL} | Reference Clock Pulse Width, LOW | | 18.5 | | ns |
| t _{PWHS} | VGAHS Pulsewidth | 2 | | | µs |
| t _{VS-HS} | VGAVS to VGAHS Delay | 0 | | | ns |
| t _S | Control Input Pulse Width, HIGH | | 50 | | ns |
| t _H | Control Input Pulse Width, LOW | | 50 | | ns |
| V _{RT} | Reference Voltage, Top | 0.5 | 0.85 | 2.0 | V |
| V _{IN} | Analog Input Range | 0 | | V _{RT} | V |
| V _{REF} | External Reference Voltage | | 1.235 | | V |
| I _{REF} | D/A Converter Reference Current (I _{REF} = V _{REF} /R _{REF} , flowing out of the R _{REF} pin) | | 3.15 | | mA |
| R _{REF} | Reference Resistor, V _{REF} = Nom | | 392 | | Ω |
| R _{OUT} | Total Output Load Resistance | | 37.5 | | Ω |
| V _{IH} | Input Voltage, Logic HIGH | 2.0 | | | V |
| V _{IL} | Input Voltage, Logic LOW | | | 0.8 | V |
| I _{OH} | Output Current, Logic HIGH | | | -2.0 | mA |
| I _{OL} | Output Current, Logic LOW | | | 4.0 | mA |
| T _A | Ambient Temperature, Still Air | 0 | | 70 | °C |
| T _C | Case Temperature, Still Air | 30 | | 105 | °C |

Electrical Characteristics

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|-----------------------------------|--|---------|-------|----------|
| I _{DD} | Power Supply Current, Operating | | 300 | 400 | mA |
| I _{DDSV} | S-Video Active | | 250 | 350 | mA |
| I _{DDCV} | Composite Video Active | | 200 | 270 | mA |
| I _{DDS} | Standby | | 80 | | mA |
| I _{DDQ} | Power Supply Current, Power-Down | | 5 | | mA |
| V _{RO} | Voltage Reference Output | 0.988 | 1.235 | 1.482 | V |
| Z _{RO} | V _{REF} Output Impedance | | 3 | | KΩ |
| C _{AI} | Input Capacitance, A/D | ADCLK = LOW ADCLK = HIGH | 4 12 | | pF pF |
| R _{IN} | Input Resistance | 500 | 1000 | | KΩ |
| I _{CB} | Input Current, Analog | | | ±15 | μA |
| C _I | Digital Input Capacitance | | 5 | 10 | pF |
| C _O | Digital Output Capacitance | | 10 | | pF |
| I _{IH} | Input Current, HIGH | V _{DD} = Max, V _{IN} = V _{DD} | | ±10 | μA |
| I _{IL} | Input Current, LOW | V _{DD} = Max, V _{IN} = 0 V | | ±10 | μA |
| I _{OS} | Short-Circuit Current | | -20 | -80 | mA |
| V _{OH} | Output Voltage, HIGH | I _{OH} = Max | 2.4 | | V |
| V _{OL} | Output Voltage, LOW | I _{OL} = Max | | 0.4 | V |

Switching Characteristics

| Parameter | Conditions | Min | Typ | Max | Units |
|------------------|-----------------------------|-----|-----|-----|-------|
| t _{DS} | Sync Output Delay | | 100 | | ns |
| t _{DOV} | Analog Output Delay | | | 15 | ns |
| t _R | D/A Output Current Risetime | | 2 | | ns |
| t _F | D/A Output Current Falltime | | 2 | | ns |

Input System Performance Characteristics

| Parameter | Conditions | Min | Typ | Max | Units | |
|-----------------|---|--|------|------|-------|----|
| E _{LI} | A/D Integral Linearity Error, Independent | | ±0.3 | ±0.5 | LSB | |
| E _{LD} | A/D Differential Linearity Error | | ±0.3 | ±0.5 | LSB | |
| E _{AP} | Aperture Error | | 30 | | ps | |
| E _{OT} | Offset Voltage, Top | R _T - V _{IN} for most positive code transition | -20 | 45 | 80 | mV |
| E _{OB} | Offset Voltage, Bottom | V _{IN} for most negative code transition | 30 | 65 | 110 | mV |

Note: Values shown in Typ column are typical for V_{DD} = V_{DDA} = +5V and T_A = 25°C.

Output System Performance Characteristics

| Parameter | | Conditions | Min | Typ | Max | Units |
|-----------|------------------------------|--------------------------------------|-----|-----|-------|------------------------|
| RES | D/A Converter Resolution | | 9 | 9 | 9 | Bits |
| dp | Differential Phase | PXCK = 27 MHz, 40 IRE Ramp | | 0.5 | | degree |
| dg | Differential Gain | PXCK = 27 MHz, 40 IRE Ramp | | 1.5 | | % |
| CNLP | Chroma Nonlinear Phase | NTC-7 Combination | | | ±1.25 | degree |
| CNLG | Chroma Nonlinear Gain | NTC-7 Combination | | | ±1.0 | % |
| PSRR | Power Supply Rejection Ratio | C _{BYP} = 0.1 μF, f = 1 KHz | | 0.5 | | %/ %V _{DD} |

Notes:

1. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode".

Table 16. MQFP Package - Pin Assignments

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------------------|-----|--------------------|-----|-------------------|-----|---------------------|
| 1 | AGND | 21 | DGND | 41 | PAL800 | 61 | DGND |
| 2 | COMPOSITE | 22 | DGND | 42 | FIL | 62 | V _{DD} |
| 3 | R _{REF} | 23 | DGND | 43 | DPMS | 63 | AGND |
| 4 | V _{REF} | 24 | DGND | 44 | VSCOM | 64 | LPF _D |
| 5 | DGND | 25 | DGND | 45 | VGAVS | 65 | V _{DDPLL} |
| 6 | PHASE | 26 | VSOUT | 46 | VGAHS | 66 | AGND |
| 7 | V _{DD} | 27 | HSOUT | 47 | POS _R | 67 | LPF _E |
| 8 | DGND | 28 | DGND | 48 | POS _D | 68 | V _{DDPLLE} |
| 9 | V _{DD} | 29 | V _{DD} | 49 | AGND | 69 | XTAL ₂ |
| 10 | DGND | 30 | DGND | 50 | B | 70 | XTAL ₁ |
| 11 | 27MHz | 31 | A1 | 51 | V _{DDA} | 71 | RESET\ |
| 12 | PXCK | 32 | A0 | 52 | V _{DDA} | 72 | PWRDN\ |
| 13 | ADCLK | 33 | V _{DD} | 53 | G | 73 | SVIDEN |
| 14 | V _{DD} | 34 | V _{DD} | 54 | AGND | 74 | CVIDEN |
| 15 | DGND | 35 | V _{DD} | 55 | V _{RT} | 75 | V _{DDA} |
| 16 | ADIVN | 36 | DGND | 56 | V _{TOUT} | 76 | V _{DDA} |
| 17 | PDIVM | 37 | BLUE | 57 | V _{TIN} | 77 | C _{BYPR} |
| 18 | DGND | 38 | BLANK | 58 | AGND | 78 | CHROMA |
| 19 | DGND | 39 | TVSTD ₁ | 59 | R | 79 | AGND |
| 20 | DGND | 40 | TVSTD ₀ | 60 | V _{DDA} | 80 | LUMA |

Figure 3. 80 Lead Metric Quad Flat Pack (MQFP) Outline

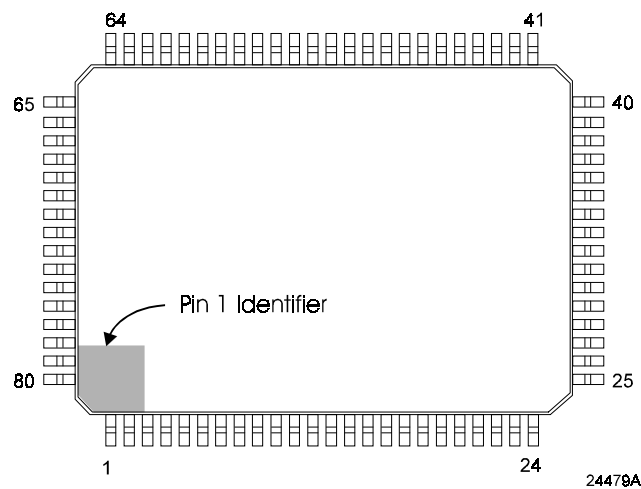


Table 17. PLCC Package - Pin Assignments

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|-------------------|-----|-----------------|-----|--------------------|-----|---------------------|
| 1 | PWRDN\ | 22 | ADCLK | 43 | A0 | 64 | G |
| 2 | SVIDEN | 23 | V _{DD} | 44 | V _{DD} | 65 | AGND |
| 3 | CVIDEN | 24 | DGND | 45 | V _{DD} | 66 | V _{RT} |
| 4 | V _{DDA} | 25 | ADIVN | 46 | V _{DD} | 67 | V _{TOUT} |
| 5 | V _{DDA} | 26 | PDIVM | 47 | DGND | 68 | V _{TIN} |
| 6 | C _{BYPR} | 27 | DGND | 48 | BLUE | 69 | AGND |
| 7 | CHROMA | 28 | DGND | 49 | BLANK | 70 | R |
| 8 | AGND | 29 | DGND | 50 | TVSTD ₁ | 71 | V _{DDA} |
| 9 | LUMA | 30 | DGND | 51 | TVSTD ₀ | 72 | DGND |
| 10 | AGND | 31 | DGND | 52 | PAL800 | 73 | V _{DD} |
| 11 | COMPOSITE | 32 | NC. | 53 | FIL | 74 | DNC |
| 12 | R _{REF} | 33 | NC. | 54 | DPMS | 75 | DNC |
| 13 | V _{REF} | 34 | DGND | 55 | VSCOM | 76 | AGND |
| 14 | DGND | 35 | DGND | 56 | VGAVS | 77 | LPF _D |
| 15 | PHASE | 36 | DGND | 57 | VGABS | 78 | V _{DDPLLD} |
| 16 | V _{DD} | 37 | VSOUT | 58 | POS _R | 79 | AGND |
| 17 | DGND | 38 | HSOUT | 59 | POS _D | 80 | LPF _E |
| 18 | V _{DD} | 39 | DGND | 60 | AGND | 81 | V _{DDPLLE} |
| 19 | DGND | 40 | V _{DD} | 61 | B | 82 | XTAL ₂ |
| 20 | 27MHz | 41 | DGND | 62 | V _{DDA} | 83 | XTAL ₁ |
| 21 | PXCK | 42 | A1 | 63 | V _{DDA} | 84 | RESET\ |

Figure 4. 84 Lead Plastic Leadless Chip Carrier (PLCC) Outline

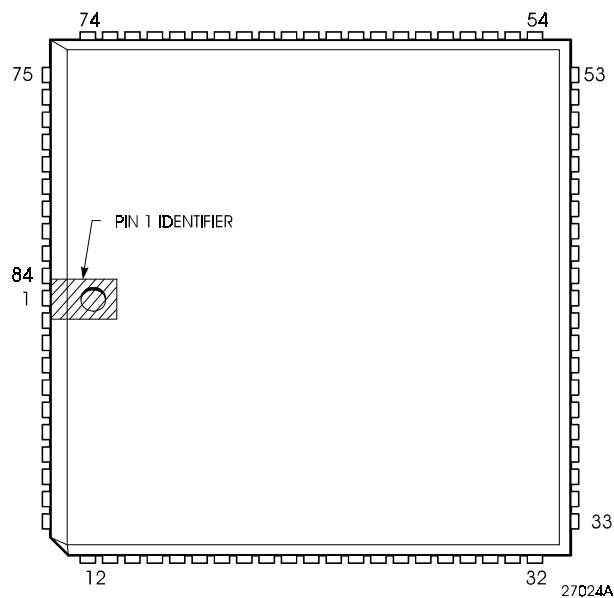


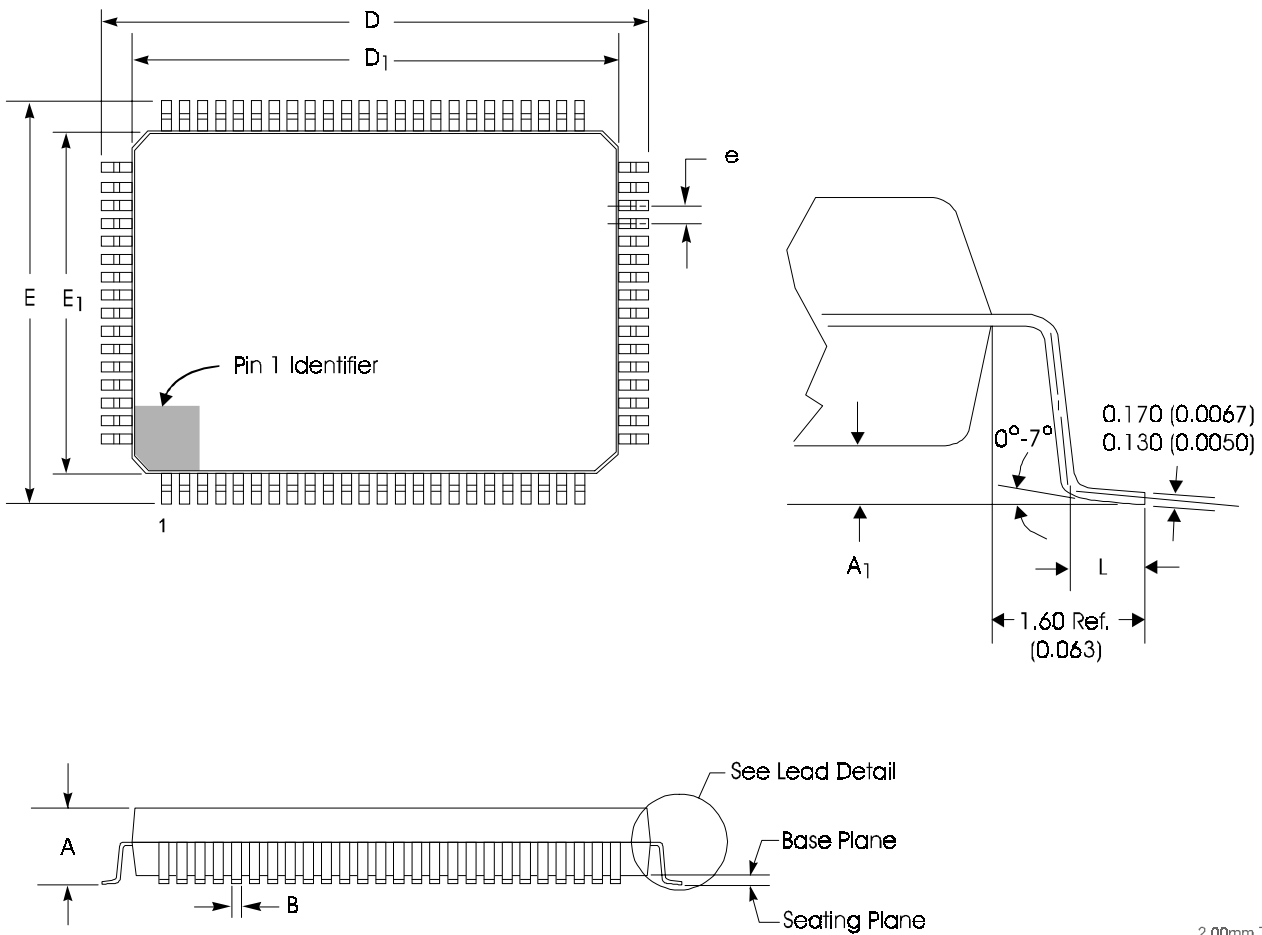
Figure 5. AIT1108KMC 80-Lead Metric Quad Flat Pack (MQFP) Dimensions

- Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
 2. Dimensions D_1 and E_1 do not include mold protrusion. Allowable protrusion is 0.010 inch (0.245 mm)
 3. Pin 1 identifier is optional.
 4. Dimension N: number of terminals.
 5. Dimensions ND, NE: number of terminals per package edge.
 6. Controlling dimension: mm.

Dimensions

| Millimeters (Inches) | | | |
|----------------------|---------------|---------------|-------------------|
| Sym | Min | Max | Notes |
| A | | 2.35 (0.093) | |
| A_1 | 0.25 (.010) | | |
| B | 0.30 (.012) | 0.40 (.0157) | |
| D | 22.95 (0.904) | 23.45 (0.923) | |
| D_1 | 19.90 (0.783) | 20.10 (0.791) | Note 2 |
| E | 16.95 (0.667) | 17.45 (0.687) | |
| E_1 | 13.90 (0.547) | 14.10 (0.555) | Note 2 |
| e | | | 0.80 (.032) Basic |
| L | 0.65 (.026) | 0.95 (.037) | |
| N | | | 80, Note 4 |
| ND | | | 24, Note 5 |
| NE | | | 16, Note 5 |

Ref. 90X00181



2.00mm Thin MQFP

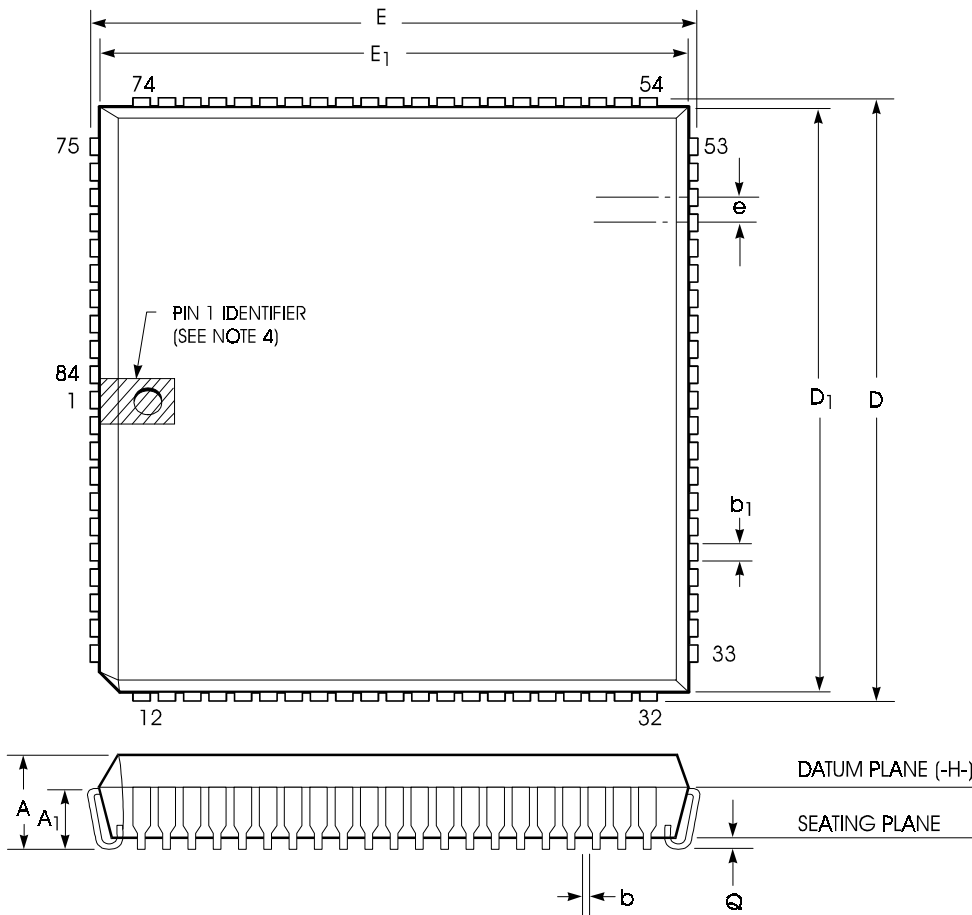
Figure 6. AIT1108R0C 84-Lead Plastic J-Leaded Chip Carrier (PLCC) Dimensions

- Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
 2. Datum plane (-H-) located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
 3. Dimensions D_1 and E_1 do not include mold protrusion. Allowable protrusion is 0.010 inch (0.245 mm)
 4. Pin 1 Identifier is optional.
 5. Dimension N: number of terminals.
 6. Dimension ND: number of terminals per package edge.
 7. Controlling dimension; mm.

Dimensions

| Inches (Millimeters) | | | |
|----------------------|---------------|---------------|-------------------|
| Sym | Min | Max | Notes |
| A | .165 (4.20) | .200 (5.08) | |
| A ₁ | .090 (2.29) | .130 (3.30) | |
| b | .013 (0.33) | .021 (0.53) | |
| b ₁ | .026 (0.66) | .032 (0.81) | |
| D | 1.185 (30.10) | 1.195 (30.35) | |
| D ₁ | 1.150 (29.21) | 1.158 (29.41) | Note 3 |
| E | 1.185 (30.10) | 1.195 (30.35) | |
| E ₁ | 1.150 (29.21) | 1.158 (29.41) | Note 3 |
| e | | | .050 (1.27) Basic |
| N | | | 84, Note 5 |
| ND | | | 21, Note 6 |
| Q | .020 (0.51) | | |

Ref. 90X00181



7356A